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Doctoral Thesis

An Analytical Model for Saturation Drain Current Including the Higher Order Effect of Source and Drain Series Resistance in Sub-20 nm MOSFETs

By

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"Show me your ways, O LORD, teach me your paths; guide me in your truth and teach me, for you are God my Savior, and my hope is in you all day long."

Psalms 25:4-5

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Abstract

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In device design of sub-20 nm metal-oxide-semiconductor field-effect transistors (MOSFETs), an accurate analytical current model including an effect of source and drain series resistance becomes important. To investigate the effects of the series resistance, the current driving capability is calculated for planar bulk, fully-depleted silicon-on-insulator (FD SOI), and multigate (MG) MOSFETs using the international technology roadmap for semiconductors (ITRS) data. We find that the effect of the series resistance becomes larger year by year, and the change of the resistance effect due to the structure change is small.

An analytical model for saturation drain current including the higher order terms of the series resistance effect is derived to improve the accuracy of the model and understand the physical meaning of the effect of higher-order terms, and simulated. As a result, the higher order terms are important for analyzing the effect of the series resistance as gate length decreases. The resistance ratio of the source resistance to the channel resistance is dominant factor in device design for sub-20 nm MOSFETs.

We investigate the structural dependence of the series resistance on saturation drain current in sub-20 nm technology nodes. The reduction rate of the saturation drain current due to the effect of the series resistance is calculated in planar bulk, FD SOI, and MG MOSFETs in high-performance (HP), low-operating-power (LOP), and low-standby-power (LSTP) technologies. We know that the reduction rate of the saturation drain current depends on the structure change of MOSFET. The dominant factor for the reduction rate of saturation drain current is the ratio of the series resistance to the channel resistance in HP technology. The dominant factor for the reduction rate of saturation drain current is the ratio of the overdrive voltage to the supply voltage in LOP technology. The dominant factor for the reduction rate of saturation drain current is the resistance and the voltage ratios in LSTP technology.

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Chapter 1

Introduction

1.1 MOSFET Miniaturization

Very-large-scale integration (VLSI) technology has been evaluated and developed to get the benefits of miniaturization such as higher density, higher circuit speed, and lower power dissipation. To evaluate and develop VLSI technology, the scaling of metal-oxide-semiconductor field-effect transistor (MOSFET) is indispensable as a part of complementary metal–oxide–semiconductor (CMOS). MOSFET miniaturization has focused on short channel effects (SCEs) and gate controllability to get required performance for scaled MOSFETs.

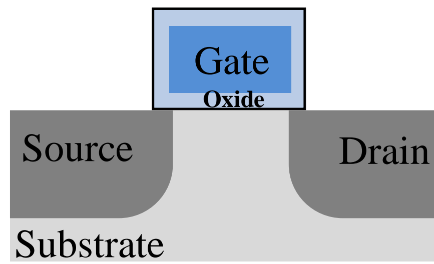
We discuss the SCEs according to MOSFET miniaturization. The scaling down to several-micrometers channel-length MOSFETs is possible by development of process techniques such as lithography and ion implant. Below sub-micro channel length, the barrier height in channel region is lowered even more when a high voltage is applied to a drain electrode, resulting in further decrease of the threshold voltage.[1] This effect is called drain-induced barrier lowering (DIBL). Due to DIBL, the threshold voltage exponentially drops as a channel length shrinks.[2] DIBL is one of SCEs. SCEs lead to deteriorate the characteristics of MOSFET, the suppressing of SCEs is an indispensable problem to improve transistor performance in device design. In device design, the structure of MOSFET is optimized to keep SCEs under control at very small regime. A kind of the method to keep SCEs under control was proposed by scaling down the vertical dimensions (gate oxide thickness, junction depth, etc.) along with the horizontal dimensions, while also proportionally decreasing the applied voltages and increasing the substrate doping concentration (decreasing the depletion width).[3, 4] For 1 μm channel length MOSFETs, the constant scaling theory introduced by R. H. Dennard.[5] Below

1 micrometer level, the constant scaling theory was not allowed by the threshold fluctuation problem due to the temperature variation of threshold voltage and SCE problem due to the nonscalability of the junction built-in potential. To address these problems, the generalized scaling theory using the electric field scaling parameter was proposed for a quarter micrometer MOSFET.[6] In addition, there are problems associated with the with electric fields that occur in short channel devices, namely reduced avalanche breakdown voltage. At sub-micro regime, while the halo doping can be used to improve the device threshold and punch through behavior, it can also cause the peak drain electric field to increase and thus decrease the breakdown voltage.[7] The threshold voltage can be adjusted by channel doping such as uniform channel doping and retrograde channel doping. These doping technics in channel region have some disadvantages. The disadvantages are the degradation of the carrier mobility in channel region and the increase of the subthreshold leakage. To alleviate the mobility degradation, high mobility materials such as strained Si, InGaAs, and Ge are proposed.[8] Moreover, when voltage is applied to the drain electrode, a high electrical field is generated in the drain region.[9] As carriers pass this region, carriers gain energy from the electrical field and become hot carriers. Some hot carriers are injected into the gate oxide. The other carriers generate electron-hole pair by impact ionization and some generated carriers flow substrate. This phenomenon changes the threshold voltage and the transconductance. To avoid this phenomenon, lightly doped drain (LDD) technique was used. Due to LDD structure, impact ionization in the channel is decreased, which reduces substrate hole current and hot electron-induced threshold voltage instability.[10]

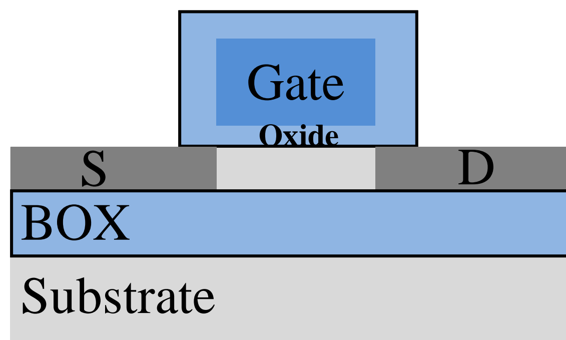
We discuss the gate controllability on MOSFET miniaturization. Since the gate has a better control to the channel, the thickness of the gate oxide also needs to be scaled when the gate length is scaled.[11] In 100 nm gate length MOSFET, the thin gate oxide below 2 nm leads to increase the tunneling leakage current such as gate-source, gate-drain, and gate-substrate leakages.[12] Moreover, dopant penetration from the poly Si gate through thin SiO_2 film occurs.[13] In order to address these issues, high-κ materials have been proposed to replace the gate oxide.[14] Many challenges with high-κ integration have included threshold voltage pinning, mobility degradation due to soft optical phonons, and poor reliability.[15–17] The structure of MOSFETs has been advanced to accomplish the intended goal as the channel length shrinks below 100 nm regime. Silicon on insulator (SOI) is proposed as a new structure of MOSFET to suppress the SCEs and substrate leakage current.[18] SOI MOSFETs are able to control SCEs through the usage of a buried oxide (BOX) layer in substrate region. As the structure changes from planar bulk MOSFET to SOI MOSFET, the key point of immunity to SCEs changed from the source and drain shallow junction to thinning of the channel region and buried oxide layer.[19] In other words, the controlled region by the gate electrode is reduced to

suppress the SCEs in SOI MOSFET. In extremely scaled MOSFET below 20 nm gate length regime, two important modification types of the classical MOSFET structure, fully depleted (FD) SOI and multi gate (MG) MOSFETs have been researched and developed. A double gate (DG) MOSFET and FinFET belong to the MG MOSFETs. The planar bulk, FD SOI, and MG MOSFETs are shown in Fig. 1.1. By using a few nm silicon film on a BOX layer as shown in Fig. 1.1b, FD SOI structure has good performance immunity to SCEs.[20, 21] In additional, lower operating voltage and lower doping concentration in channel region lead to improve mobility due to less coulomb scattering and lower vertical field in extremely scaled FD SOI MOSFET. Moreover, the thin buried oxide gives threshold voltage adjustment through controlled back gate bias for undoped body UTB FD SOI MOSFET.[22] In double gate (DG) MOSFET and FinFET, to improve gate controllability and device performance with low operating voltage more effectively, MOSFET needs to have the gates on two or more sides of the channel region as illustrated in Fig. 1.1c. It means that not only the thinning of the channel region but also the addition of the gate electrode as a controller of the channel region.

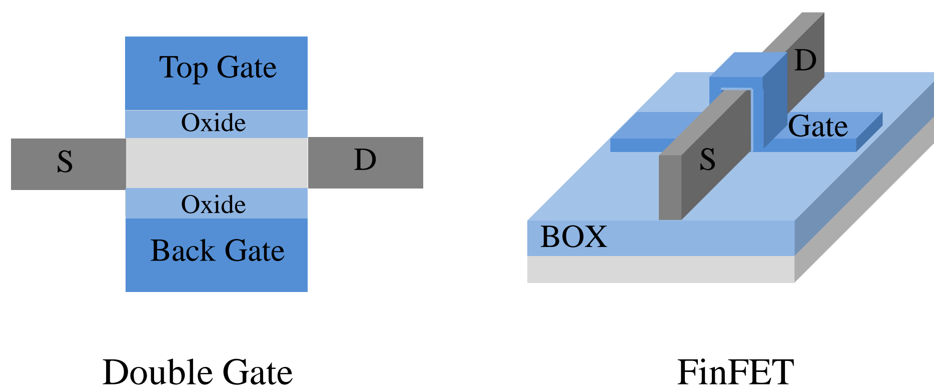
We discuss challenges of MOSFET miniaturization into nanoscale regime. Recently, namely ultra thin body (UTB) FD SOI and MG MOSFETs are proposed as the advanced MOSFET structures according to the international technology roadmap for semiconductors (ITRS) reports.[23] Actually, tri-gate MOSFET is used as 22 nm logic technology.[24] Despite the advantages of FD SOI and MG structures, there are a few challenges such as the leakage current problems[25], reliability problem due to the variation of the threshold voltage[26], and the non-negligible effect of the source and drain series resistance[27]. It is difficult to get both high performance and low leakage current despite of the change of MOSFET structure in nanoscale regime. ITRS reports have been proposed three types of CMOS device; high performance (HP), low operating power(LOP), and low standby power technologies. The HP technology uses the shortest gate length in order to achieve the higher drive current. A higher leakage current is also allowed in HP technology. To reduce the operating power of device, the LOP Technology uses a longer physical gate length and a thicker gate oxide compared to the HP technology. For the LSTP, the main target is to achieve transistors with the lowest leakage current at off state. The reliability problems have occurred by the variation of device parameters such as the threshold voltage and work function. The causes of variability are equipment stability, lithography stability, mechanical stress, and microscopic perturbation. The reducing of the source and drain series resistance is confronted with geometrical limits in the advanced MOSFETs due to the small cross sectional area of the fin extension to connect the channel and the source or drain regions.[28] In addition,



(A) Planar Bulk MOSFET



(B) FD SOI MOSFET



(C) MG MOSFET

Figure 1.1: Structures of the conventional and advanced MOSFETs. (A) Planar Bulk, (B) FD SOI, and (C) MG MOSFETs; DG MOSFET and FinFET.

extremely scaled devices are operated in low supply voltage to minimize the power consumption. The effect of the source and drain series resistance becomes a non-negligible factor in the device design. We focused on this unavoidable problem in sub-20 nm advanced MOSFETs.

1.2 Source and Drain Series Resistance

Source and drain series resistance is the resistance in source and drain regions and around their regions such as interface between source (or drain) and metal for transmission line in circuits and overlap region between the gate and source (or drain) region. In a conventional MOSFET, source and drain series resistance can be divided into four components as illustrated in Fig. 1.2.[29] In Fig. 1.2, R_{co} is contact resistance, R_{sh} is sheet resistance of the source and drain region where the current flows uniformly, R_{sp} is spreading resistance, and R_{ac} is accumulation resistance. The contact resistance is the resistance in interface region between source-drain and the top metal (or silicide). The sheet resistance is the resistance of source and drain region where the current flows uniformly. The spreading resistance is associated with current spreading from the surface layer into a uniform pattern across the depth of the source-drain. The accumulation resistance is the resistance in the gate-source (or -drain) overlap region where the current mainly stays at the surface.

According to scaling down the gate length, the junction depth of the source and drain has also to be reduced in concert with the other dimensions to control SCEs.[30] In submicrometer gate length regime, there exists an unavoidable intrinsic series resistance associated with the structure of MOSFET because this resistance is not scaled down proportionally with device size.[31] It is important to reduce the series resistance in several structure such as LDD, extended source drain since this resistance has direct influence on the current-voltage characteristics of MOSFET. LDD structure is proposed to suppress the hot carrier effect.[32] LDD structure leads to increase the resistance in drain region.[33] Device performance influenced by SCEs is improved but the source and drain series resistance becomes increasingly important due to very shallow source and drain junctions.[34] The extended source and drain have used to improve SCEs and decrease the series resistance. In the extended source and drain structure, the source and drain series resistance can be divided into four components as illustrated in Fig. 1.3. In this structure, the series resistance is added source and drain extension resistance and the spreading resistance due to the extended region as compared to the planar bulk structure. The series resistance in the extended source and drain and LDD structure is

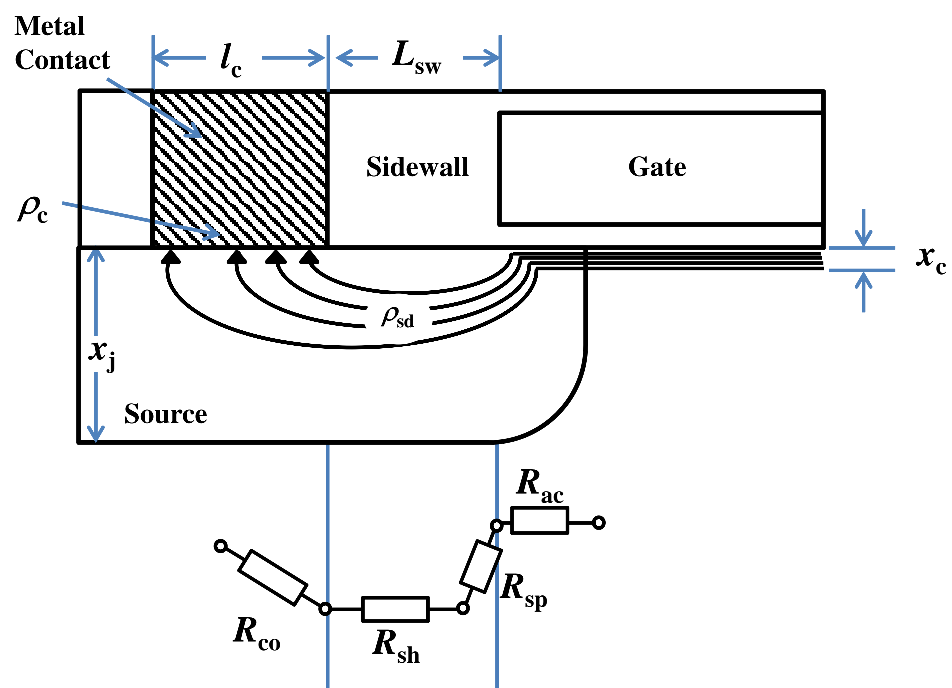


FIGURE 1.2: Schematic representation of source structure and the series resistance components in the planar bulk MOSFET.

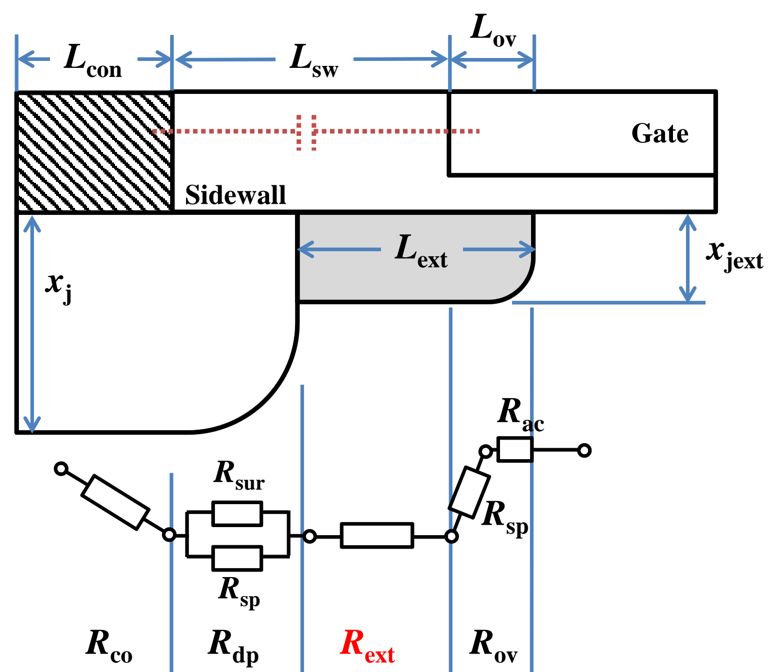


FIGURE 1.3: Simple schematic representation of source structure and the series resistance components in the extended source and drain structure.

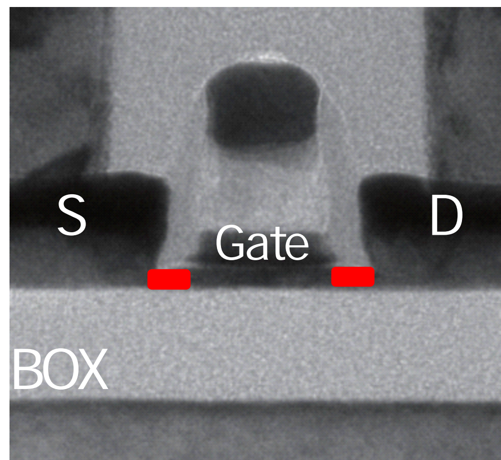
partially due to silicon properties such as the solid solubility of dopants, and some technological limitations such as the non-abrupt junction profile of the source and drain.[29] This issue is progressed by adopting raised source/drain due to the improvement of thin film deposition technique such as atomic layer deposition (ALD).[35] However, in advanced MOSFET, this technique does not work owing to small cross sectional area of the source and drain extension.

To get required performance in extremely scaled MOSFETs, the structure of MOSFET is changed from the conventional MOSFET to FD SOI and MG MOSFETs as illustrated in Fig. 1.4. Figure 1.4 shows experimental structures of the advanced MOSFETs. The marked regions in red are the extended source and drain regions for connection between source (or drain) and the channel regions in all structures in Fig. 1.4. FD SOI and DG MOSFET contain the extremely thin extended source and drain regions due to small thickness of SOI (T_{SOI}). In tri-gate FET or fin field-effect transistor (FinFET), the tall and narrow extended source and drain regions are formed to get a high device performance. These extend regions in the advanced MOSFET lead to a higher source and drain series resistance due to the bottleneck effect in these regions. In FD SOI MOSFET, the source and drain series resistance can be divided into four components as illustrated in Fig. 1.5. A thin channel region used for good short channel control results in a larger source and drain series resistance due to small cross sectional area of the source and drain extension. The length of the extended regions is increased by the augment of the sidewall length (L_{sw}) due to reducing of the capacitance between the gate and source. In MG MOSFETs, the source and drain series resistance can be divided into four components as illustrated in Fig. 1.6. Moreover, the power supply voltage reduces to reduce power consumption. Therefore, the impact of the series resistance on drain current becomes non-negligible factor in a sub-20nm gate length regime. To consider this problem, the series resistance effect is modeled in the drain current models.

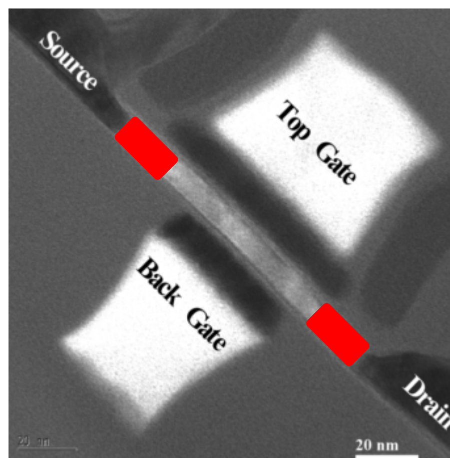
1.3 Analytical Drain Current Model

There are numerical current model and analytical current model for MOSFET. The numerical current model provides precise solutions from complicated equations by using a computer. On the other hand, analytical current model for MOSFET consists of physical parameters such as voltages, lengths, velocities, mobility, and so on. It provides a simple way to understand, analyze, and design MOSFET.

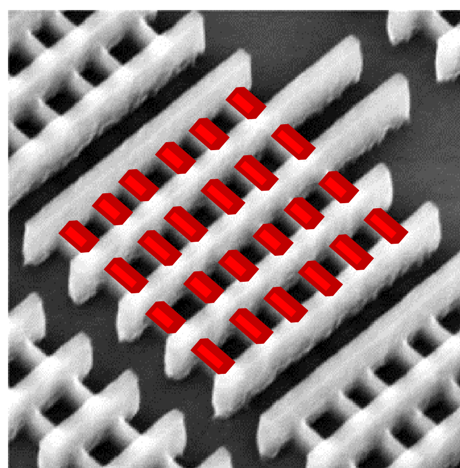
A physically based continuous short-channel model was proposed including the effects of the channel length modulation, DIBL, low field surface mobility, the source and drain



(A) FD SOI MOSFET[36]



(B) DG MOSFET[37]



(C) Tri-Gate FET[38]

FIGURE 1.4: Experimental Structures of the advanced MOSFETs. (A) FD SOI MOSFET, (B) DG MOSFET, and (C) Tri-Gate MOSFET.

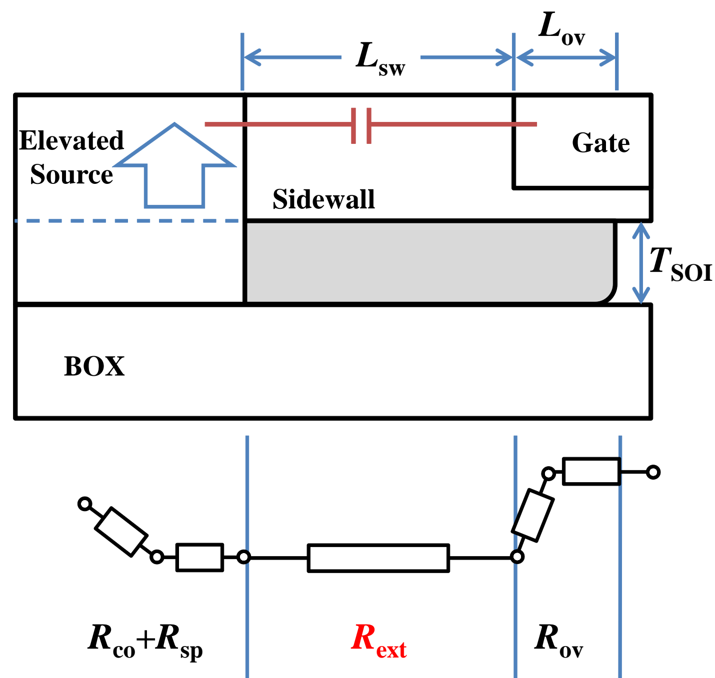


FIGURE 1.5: Schematic representation of source structure and the series resistance components in FD SOI MOSFET.

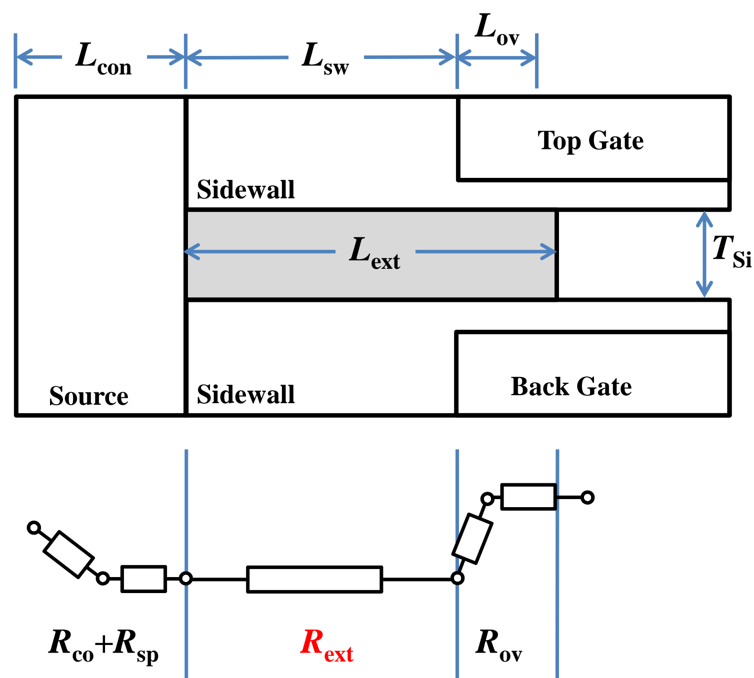


FIGURE 1.6: Schematic representation of source structure and the series resistance components in MG MOSFET.

resistance, and impact ionization current for deep sub-micron MOSFET.[39] In this model, inclusion of the source and drain series resistance is possible through the mobility term[40]. However, this procedure of including the series resistance through mobility becomes poor as the resistance is above 150-200 Ω owing to the used assumption. Therefore, the mobility term in this model can be partially accepted to apply to more shorter gate length MOSFET.[41]

An engineering model included the effects of velocity saturation, and gate-threshold voltages independent was proposed for several micrometers of gate-length MOSFETs.[42] This saturation drain current was modified to consider the effects of source and drain series resistance in deep submicrometer for LDD MOSFET.[43] A semi-empirical saturation drain current model[44] was proposed including an empirical mobility models[45]. For extremely scaled device, an empirical mobility model and SCEs such effects as DIBL, channel-length modulation (CLM), avalanche enhanced body effect (AEBE), and substrate leakage current in the saturation current and the threshold voltage[46] are added.[47] This model was modified again to include structure dependence for FD SOI and MG MOSFETs.[48] This model has used in ITRS technical reports as a model for assessment of CMOS technologies and roadmaps (MASTAR).[49] However, it is difficult from this model owing to information lack of the series resistance effects to understand and analyze accurate effects of source and drain series resistance for extremely scaled device. It is necessary to optimize and design for low power device. Therefore, the saturation drain-current model including the higher order effect of the source and drain series resistance becomes important in a sub-20nm gate length regime.

1.4 Purpose of this work and Organization

The purpose of this work is to give feedback on device design for sub-20 nm advanced MOSFETs by analysis results of the device simulation. The device simulation is based on analytical drain-current model. We will investigate the effect of the source and drain series resistance on device characteristics and parameters of the drain-current model in the saturation region to clarify the resistance effect on future devices. To improve an accuracy of the drain-current model, a saturation current model including the high order effect of the source and drain series resistance will be derived. It provides the understanding of physical meaning of effect of the series resistance, and the direction of device optimization and development through the analysis of an analytical model derived here. Sub-20 nm planar bulk, FD SOI, and MG MOSFETs apply to derived model in HP, LOP, and LSTP technologies.

This thesis has been organized into six chapters.

Chapter 2 focuses on the analytical saturation drain-current models. We introduce the past analytical models including the effect of the series resistance. Then, analytical model including higher order effects of the series resistance for saturation drain current is derived. We briefly introduce the α power model used for circuit simulation.

In Chapter 3, the effects of source and drain series resistance on device characteristics are investigated for sub-20 nm MOSFETs. The current driving capability is calculated for several structures such as planar bulk, FD SOI, and MG MOSFETs by using the ITRS data. In order to investigate the effects of source and drain series resistance on the device parameters such as the channel length modulation coefficient and the saturation drain current, the drain current is simulated by using the circuit simulation.

In Chapter 4, we discuss a reduction in saturation drain current by the source and drain series resistance in the sub-20 nm technology node. To improve the accuracy of the model and understand the physical meaning of the effect of higher-order terms, an analytical saturation drain current model including an effect of higher-order terms of the series resistance will be derived, and simulated using ITRS data. Through the analysis of the results, an effect of higher-order terms of the saturation drain current and the relationships between physical parameters and the current reduction will be discussed.

In Chapter 5, we investigate the structural dependence of the source-and-drain series resistance on saturation drain current for planer bulk, SOI, and MG MOSFETs in sub-20 nm technology nodes. To investigate the structural dependence, the reduction rate of the saturation drain current due to the effect of the series resistance is calculated in CMOS logic technologies. The reduction rates and expansion components of the saturation drain current are discussed to clarify the relationships between physical parameters and the current reduction.

Finally, the key points of this dissertation are summarized in Chapter 6.

Chapter 2

Analytical Model for Saturation Drain Current

This chapter begins with an introduction of the past analytical models including the effect of the series resistance. Then, analytical model including higher order effects of the series resistance for saturation drain current will be derived in section 2.2. To investigate the effect of the series resistance on model parameters by circuit simulation, a simple current model for circuit simulation is used the α power model. This model will be introduced in section 2.3.

2.1 Analytical Current Model Including the Effect of the Series Resistance

An engineering model was proposed for several micrometers of gate-length MOSFETs. [42] This analytical current model includes the effects of velocity saturation, and gate-threshold voltages independently. The drain current of this analytical current model in the saturation region can be shown:

$$I_{\mathrm{Dsat0}} = \frac{\nu_{\mathrm{sat}} C_{\mathrm{ox}} W (V'_{\mathrm{GS}} - V_{\mathrm{T}})}{1 + E_{\mathrm{c}} L_{\mathrm{e}} / (V'_{\mathrm{GS}} - V_{\mathrm{T}})}, \tag{2.1}$$

where

$$E_{\mathrm{c}} = \frac{2\nu_{\mathrm{sat}}}{\mu_{\mathrm{eff}}}, \tag{2.2}$$

where ν_{sat} is saturation velocity, C_{ox} is gate capacitance per unit area, W is device width, V'_{GS} is gate to source voltage without the effect of source and drain series resistance, V_{T} is the device threshold voltage, and L_{e} is the device electrical channel length. This

saturation drain current was modified to consider the effects of source and drain series resistance in deep submicrometer for LDD MOSFET.[43] To consider dependence of gate voltage, body bias, gate oxide thickness, and channel doping concentration, an empirical mobility model[45] was proposed using a single parameter as follows:

$$\mu_{\text{eff}} = \frac{540}{1 + \left(\frac{E_{\text{eff}}}{0.9}\right)^{1.85}}, \tag{2.3}$$

A semi-empirical saturation drain current model[44] was proposed including the empirical mobility model. Moreover, this semi-empirical model includes the first order Taylor expansion of source and drain series resistance using $V'_{\text{GS}} = V_{\text{GS}} - I_{\text{Dsat}}R_{\text{s}}$ according to the equivalent circuit in Fig. 2.1 as follows:

$$I_{\text{Dsat}}(R_{\text{s}}) = I_{\text{Dsat0}}\left(1 - \frac{2I_{\text{Dsat0}}R_{\text{s}}}{V_{\text{GS}} - V_{\text{T}}} + \frac{I_{\text{Dsat0}}R_{\text{s}}}{V_{\text{GS}} - V_{\text{T}} + E_{\text{sat}}L_{\text{eff}}}\right), \tag{2.4}$$

where, I_{Dsat0} is the saturation current in Eq. (2.1) when source series resistance R_{s} is 0, E_{sat} is vertical channel field, L_{eff} is the channel length, V'_{GS} is gate to source voltage including the effect of source and drain series resistance, and V_{T} is the threshold voltage. In the range of 0.025 - 0.5 μm gate length, it is necessary to consider mobility degradation due to doping concentration in channel region and SCEs such effects as DIBL, channel-length modulation (CLM), narrow channel effect (NCE) avalanche enhanced body effect (AEBE), and substrate leakage current in the saturation current and the threshold voltage. The drain current model for saturation region was introduced including these effects as follows:[48]

$$I_{\text{Dsat}} = \frac{I_{\text{Dsat0}}}{1 - \frac{2I_{\text{Dsat0}}R_{\text{s}}}{V_{\text{GS}} - V_{\text{th,on}}} + \frac{I_{\text{Dsat0}}R_{\text{s}}}{V_{\text{GS}} - V_{\text{th,on}} + E_{\text{c}}L_{\text{el}}(1+d)}}, \tag{2.5}$$

$$I_{\text{Dsat0}} = \frac{1}{2}\mu_{\text{eff}}C_{\text{oxel}}\frac{(V'_{\text{GS}} - V_{\text{th,on}})^2 E_{\text{c}}}{(V'_{\text{GS}} - V_{\text{th,on}}) + L_{\text{el}}E_{\text{c}}(1+d)}, \tag{2.6}$$

$$d = \frac{qN_{\text{ch}}\sqrt{2\varepsilon_{\text{Si}}(2\phi_{\text{F}} - V_{\text{b}})/qN_{\text{ch}}}}{2C_{\text{oxel}}(2\phi_{\text{F}} - V_{\text{b}})}, \tag{2.7}$$

$$2\phi_{\text{F}} = \frac{kT}{q}\ln\left(\frac{N_{\text{ch}}}{n_{\text{i}}}\right)^2, \tag{2.8}$$

$$C_{\text{oxel}} = \frac{\varepsilon_{\text{SiO2}}}{T_{\text{oxel}}}, \tag{2.9}$$

$$T_{\text{oxel}} = T_{\text{phys}}\frac{\varepsilon_{\text{SiO2}}}{\varepsilon_{\text{actual}}} + D_{\text{arkspace}} + P_{\text{olydepl}}, \tag{2.10}$$

where $V_{\text{th,on}}$ is threshold voltage including the SCEs, L_{el} is electric gate length, E_{c} is electric field corresponding to velocity saturation voltage as in Eq. (2.2), R_{sd} is the

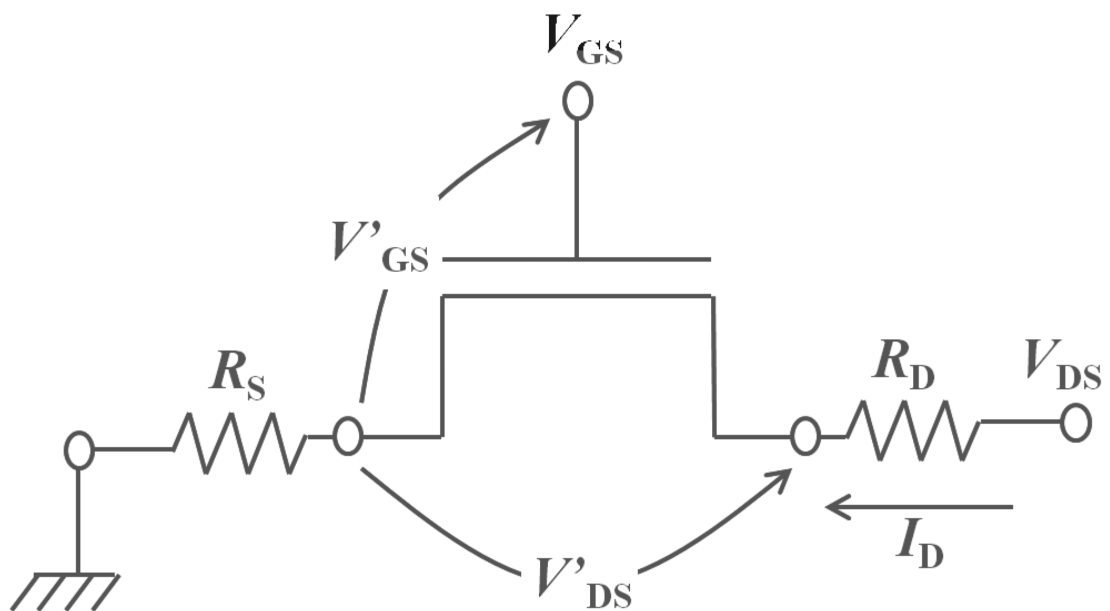


FIGURE 2.1: Equivalent circuit including the intrinsic MOSFET and the series resistance.

source series resistance ($R_{\mathrm{sd}}/2 = R_{\mathrm{s}} = R_{\mathrm{d}}$), q is the electric charge, k is the Boltzmann constant, T is absolute temperature, $\varepsilon_{\mathrm{Si}}$ is the silicon permittivity, $\varepsilon_{\mathrm{SiO2}}$ is the silicon oxide permittivity, $\varepsilon_{\mathrm{actual}}$ is the permittivity of high-κ material as a gate oxide, V_{b} is an applied substrate voltage, N_{ch} is channel doping concentration, n_{i} is intrinsic carrier concentration, and T_{phys} is thickness of high-κ material as a gate oxide. To consider the effective gate length including the quantum effect, dark space D_{arkspace} is assumed as 2-4 Å. Poly depletion P_{olydepl} is assumed as 4 Å. This model has used in model for assessment of CMOS technologies and roadmaps (MASTAR).[49] To consider mobility degradation, an actual effective mobility[47] takes into account acoustic phonon and surface roughness effects as a function of the effective transversed field at surface as follows:

$$\mu_{\mathrm{eff}} = \frac{\mu_{\mathrm{sr}}\mu_{\mathrm{ac}}}{\mu_{\mathrm{sr}} + \mu_{\mathrm{ac}}}, \tag{2.11}$$

$$\mu_{\mathrm{sr}}\left[\frac{\mathrm{cm}^2}{\mathrm{Vs}}\right] = 1450E_{\mathrm{eff}}^{-2.9}\left[\frac{\mathrm{MV}}{\mathrm{cm}}\right], \tag{2.12}$$

$$\mu_{\mathrm{ac}}\left[\frac{\mathrm{cm}^2}{\mathrm{Vs}}\right] = 330E_{\mathrm{eff}}^{-0.3}\left[\frac{\mathrm{MV}}{\mathrm{cm}}\right], \tag{2.13}$$

$$E_{\mathrm{eff}} = \frac{V_{\mathrm{GS}} + V_{\mathrm{th,on}}}{6T_{\mathrm{oxel}}} - 2\frac{V_{\mathrm{FB}} + 2\phi_{\mathrm{F}}}{6T_{\mathrm{oxel}}}. \tag{2.14}$$

To consider SCEs in short channel device, this model was developed using a threshold voltage according to the voltage-doping transformation (VDT) technique.[48, 50] The threshold voltage including the effects of reverse short-channel effect (RSCE), SCE, DIBL, CLM, and NCE can be expressed as follows:

$$V_{\mathrm{th,on}} = V_{\mathrm{th,off}} + 0.03\mathrm{V}, \tag{2.15}$$

$$V_{\mathrm{th,off}} = V_{\mathrm{th}\infty} + RSCE - SCE - DIBL - NCE, \tag{2.16}$$

$$V_{\mathrm{th}\infty} = V_{\mathrm{FB}} + 2\phi_{\mathrm{F}} + \frac{1}{C_{\mathrm{oxeot}}}\sqrt{2\varepsilon_{\mathrm{Si}}qN_{\mathrm{B}}(2\phi_{\mathrm{F}} - V_{\mathrm{BS}})}, \tag{2.17}$$

$$RSCE = \frac{\sqrt{2\varepsilon_{\mathrm{Si}}qN_{\mathrm{B}}(2\phi_{\mathrm{F}} - V_{\mathrm{BS}})}}{C_{\mathrm{ox}}}\left(\sqrt{\frac{N_{\mathrm{ch}}}{N_{\mathrm{B}}}} - 1\right), \tag{2.18}$$

$$SCE = 0.64\frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}} \times EI \times \phi_{\mathrm{d}}, \tag{2.19}$$

$$\phi_{\mathrm{d}} = \frac{kT}{q}\ln\left(\frac{N_{\mathrm{ext}}N_{\mathrm{ch}}}{{n_{\mathrm{i}}}^2}\right), \tag{2.20}$$

$$DIBL = 0.8\frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}} \times EI \times V_{\mathrm{DS}}, \tag{2.21}$$

$$NCE = \frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}}\frac{T_{\mathrm{ox}}T_{\mathrm{dep}}}{W^2}\sigma, \tag{2.22}$$

$$T_{\mathrm{dep}} = \sqrt{\frac{2\varepsilon_{\mathrm{s}}}{qN_{\mathrm{ch}}}(2\phi_{\mathrm{F}} - V_{\mathrm{b}})}, \tag{2.23}$$

$$EI = \left(1 + \frac{{X_{\mathrm{j}}}^2}{{L_{\mathrm{el}}}^2}\right)\frac{T_{\mathrm{oxel}}}{L_{\mathrm{el}}}\frac{T_{\mathrm{dep}}}{L_{\mathrm{el}}}, \tag{2.24}$$

where, N_{ext} is doping concentration in source and drain extended region.

Gate length shrinks into nanometer regime, UTB FD SOI and MG MOSFETs are proposed as the advanced MOSFET structures. In these advanced structure, effective transverse field is changed by ultra thin body and multi gate. In addition, SCEs are suppressed by changing of MOSFET structure. To take into account effects of structure change, it is necessary to modify the effective transverse field and EI. For FD SOI MOSFET, E_{eff} and EI are defined as follows:

$$E_{\mathrm{eff}} = \left(\frac{V_{\mathrm{GS}} + V_{\mathrm{T}}}{6T_{\mathrm{oxel}}} - 2\frac{V_{\mathrm{FB}} + 2\phi_{\mathrm{d}} - \Psi_{\mathrm{BOX}}}{6T_{\mathrm{oxel}}}\right), \tag{2.25}$$

$$\Psi_{\mathrm{BOX}} = \frac{qN_{\mathrm{GP}}T_{\mathrm{sub}}}{C_{\mathrm{ox}}}, \tag{2.26}$$

$$T_{\mathrm{sub}} = -(T_{\mathrm{Si}} + 3T_{\mathrm{box}}) + \sqrt{(T_{\mathrm{Si}} + 3T_{\mathrm{box}})^2 + \frac{2\varepsilon_{\mathrm{Si}}\phi_{\mathrm{d}}}{qN_{\mathrm{GP}}} - \frac{N_{\mathrm{A}}}{N_{\mathrm{GP}}}{T_{\mathrm{Si}}}^2}, \tag{2.27}$$

$$EI = \left(1 + \frac{{T_{\mathrm{Si}}}^2/2}{{L_{\mathrm{el}}}^2}\right)\frac{T_{\mathrm{oxel}}}{L_{\mathrm{el}}}\frac{T_{\mathrm{Si}} + \lambda T_{\mathrm{box}}}{L_{\mathrm{el}}}, \tag{2.28}$$

where T_{Si} is thickness of silicon body, T_{box} is thickness of buried oxide, N_{GP} is doping concentration under the BOX, and N_{A} is accepter concentration. For MG MOSFET, the effective transverse field and threshold voltage have an additional term due to coupling between both gates. E_{eff} and EI are defined as follows:

$$E_{\mathrm{eff}} = \left(\frac{V_{\mathrm{GS}} + V_{\mathrm{T}}}{6T_{\mathrm{oxel}}} - 2\frac{V_{\mathrm{FB}} + 2\phi_{\mathrm{d}} - \Psi_{\mathrm{SUP}}}{6T_{\mathrm{oxel}}}\right), \tag{2.29}$$

$$\Psi_{\mathrm{SUP}} = \phi_{\mathrm{d}} - 2\phi_{\mathrm{F}} - \frac{kT}{q}\left[\ln\left(\frac{kT}{q^2}\cdot\frac{1}{N_{\mathrm{A}}}C_{\mathrm{ox}}\mathrm{e}^{\frac{\left(\frac{q}{KT}+1\right)}{2}}\right)\right], \tag{2.30}$$

$$EI = \left(1 + \frac{{T_{\mathrm{Si}}}^2/4}{{L_{\mathrm{el}}}^2}\right)\frac{T_{\mathrm{oxel}}}{L_{\mathrm{el}}}\frac{T_{\mathrm{Si}}/2}{L_{\mathrm{el}}}. \tag{2.31}$$

For nanoscale MOSFET, the analytical model used in MASTAR includes the effect of quantum ballistic transport[51]. To reflect quasi-ballistic enhanced transport in highly scaled MOSFETs, the saturation current is multiplied by the effective ballistic enhancement factor.

2.2 Analytical Model Including the Higher Order Effect of the Series Resistance

The effect of the series resistance in saturation drain current can be examined by using an equivalent circuit in Fig. 2.1. The equivalent circuit consists of an intrinsic MOSFET, a source resistance, and a drain resistance as the series resistance. The drain current flows through the drain resistance, the channel, and the source resistance. At that time, a voltage drop occurs owing to the resistances. Therefore, internal voltages ($V'_{\mathrm{GS}}, V'_{\mathrm{DS}}$) are given by[1, 52, 53]

$$V'_{\mathrm{GS}} = V_{\mathrm{GS}} - I_{\mathrm{D}} \cdot R_{\mathrm{S}}, \tag{2.32}$$

$$V'_{\mathrm{DS}} = V_{\mathrm{DS}} - I_{\mathrm{D}} \cdot (R_{\mathrm{S}} + R_{\mathrm{D}}), \tag{2.33}$$

where R_{S} and R_{D} are the source and drain resistances per unit gate width, respectively. From Eq. (2.32), the saturation drain current is reduced by the gate-voltage drop ($I_{\mathrm{Dsat}} \cdot R_{\mathrm{S}}$) because of the source resistance. The saturation current equation solved by using the quadratic formula can be expressed as follows:

$$I_{\mathrm{Dsat}} = \frac{-B - \sqrt{B^2 - 4AC}}{2A}, \tag{2.34}$$

$$A = \frac{1}{2}\mu_{\mathrm{eff}} C_{\mathrm{ox}} E_{\mathrm{c}} R_{\mathrm{S}}^2 + R_{\mathrm{S}}, \tag{2.35}$$

$$B = -[V_{\mathrm{gt}} + L_{\mathrm{el}} E_{\mathrm{c}}(1+d) + \mu_{\mathrm{eff}} C_{\mathrm{ox}} E_{\mathrm{c}} R_{\mathrm{S}} V_{\mathrm{gt}}], \tag{2.36}$$

$$C = \frac{1}{2}\mu_{\mathrm{eff}} C_{\mathrm{ox}} E_{\mathrm{c}} V_{\mathrm{gt}}^2, \tag{2.37}$$

where V_{gt} is the overdrive voltage ($V_{\mathrm{GS}} - V_{\mathrm{th,on}}$) and I_{Dsat} is the saturation drain current per unit gate width including the effect of the series resistance. Equation (2.34) becomes complicated owing to the fact that it contains a root term. To analyze the physical meaning from the complicated form of I_{Dsat}, the Taylor expansion is used. I_{Dsat} including the higher-order terms of R_{S} can be rewritten as follows:

$$I_{\mathrm{Dsat}} = I_{\mathrm{Dsat0}}(1 + a_1 R_{\mathrm{S}} + a_2 R_{\mathrm{S}}^2 + a_3 R_{\mathrm{S}}^3 + a_4 R_{\mathrm{S}}^4 + O(R_{\mathrm{S}}^5)), \tag{2.38}$$

$$a_1 = I_{\mathrm{Dsat0}}\left(\frac{\alpha - 2}{V_{\mathrm{gt}}}\right), \tag{2.39}$$

$$a_2 = I_{\mathrm{Dsat0}}^2\left(\frac{2\alpha^2 - 6\alpha + 5}{V_{\mathrm{gt}}^2}\right), \tag{2.40}$$

$$a_3 = I_{\mathrm{Dsat0}}^3 \left(\frac{5\alpha^3 - 20\alpha^2 + 28\alpha - 14}{V_{\mathrm{gt}}^3} \right), \tag{2.41}$$

$$a_4 = I_{\mathrm{Dsat0}}^4 \left(\frac{14\alpha^4 - 70\alpha^3 + 135\alpha^2 - 120\alpha + 42}{V_{\mathrm{gt}}^4} \right), \tag{2.42}$$

$$\alpha = \frac{V_{\mathrm{gt}}}{V_{\mathrm{gt}} + L_{\mathrm{el}} E_{\mathrm{c}} (1 + d)}. \tag{2.43}$$

Equation (2.38) is the 4th-order approximated analytical current model. A 1st-order approximation of Eq. (2.34) is identical to the semiempirical saturation drain current model equation[54] in Eq. (2.4). Each term of Eq. (2.38) can be divided into three components by using a channel resistance ($R_{\mathrm{ch}} = V_{\mathrm{dd}} / I_{\mathrm{Dsat0}}$) as follows:

$$a_1 R_{\mathrm{S}} = \left(\frac{R_{\mathrm{S}}}{R_{\mathrm{ch}}} \right) \cdot \left(\frac{V_{\mathrm{dd}}}{V_{\mathrm{gt}}} \right) \cdot \Big(\alpha - 2 \Big), \tag{2.44}$$

$$a_2 R_{\mathrm{S}}^2 = \left(\frac{R_{\mathrm{S}}}{R_{\mathrm{ch}}} \right)^2 \cdot \left(\frac{V_{\mathrm{dd}}}{V_{\mathrm{gt}}} \right)^2 \cdot \Big(2\alpha^2 - 6\alpha + 5 \Big), \tag{2.45}$$

$$a_3 R_{\mathrm{S}}^3 = \left(\frac{R_{\mathrm{S}}}{R_{\mathrm{ch}}} \right)^3 \cdot \left(\frac{V_{\mathrm{dd}}}{V_{\mathrm{gt}}} \right)^3 \cdot \Big(5\alpha^3 - 20\alpha^2 + 28\alpha - 14 \Big), \tag{2.46}$$

$$a_4 R_{\mathrm{S}}^4 = \left(\frac{R_{\mathrm{S}}}{R_{\mathrm{ch}}} \right)^4 \cdot \left(\frac{V_{\mathrm{dd}}}{V_{\mathrm{gt}}} \right)^4 \cdot \Big(14\alpha^4 - 70\alpha^3 + 135\alpha^2 - 120\alpha + 42 \Big). \tag{2.47}$$

We investigate the physical meaning of the components. The first components are ratios of the source resistance to the channel resistance. The second components are ratios of the supply voltage to the overdrive voltage. The third components are functions of V_{gt}, L_{el}, E_{c}, and d. As the degrees of terms increase, the degrees of the first and second components increase. We can obtain the explicit forms of the saturation current model including the effect of the series resistance.

2.3 A Simple Analytical Current Model for Circuit Design

A simple analytical drain current model was proposed for circuit design.[55] The model can be expressed as follows:

$$I_{\mathrm{DSAT}} = \frac{W}{L_{\mathrm{EFF}}} B (V_{\mathrm{GS}} - V_{\mathrm{TH}})^n, \tag{2.48}$$

$$I_{\mathrm{D}} = I_{\mathrm{D5}} = I_{\mathrm{DSAT}} (1 + \lambda V_{\mathrm{DS}}), (V_{\mathrm{DS}} \geq V_{\mathrm{DSAT}}: \text{ Saturation Region}), \tag{2.49}$$

$$V_{\mathrm{DSAT}} = K (V_{\mathrm{GS}} - V_{\mathrm{TH}})^m, \tag{2.50}$$

$$I_{\rm D} = I_{\rm D3} = I_{\rm D5}\left(2 - \frac{V_{\rm DS}}{V_{\rm DSAT}}\right)\frac{V_{\rm DS}}{V_{\rm DSAT}}, (V_{\rm DS} < V_{\rm DSAT}\text{: Linear Region}), \tag{2.51}$$

where $L_{\rm EFF}$ is an effective channel length, $V_{\rm DSAT}$ is a drain saturation voltage, λ is a channel length modulation, parameters K and m control the linear region characteristics, and parameters B and n determine the saturated region characteristics. It expresses a current-voltage characteristic in saturation region for short-channel devices using the parameters including SCEs despite a simple form. λ is related to the finite drain conductance in the saturated region. In this thesis, this model will be used for circuit simulation instead of the analytical model introduced in section 2.2.

Chapter 3

Effects of Source and Drain Resistances on Analytical Model Parameters for 20 nm MOSFETs

Since the reduction of development costs and faster time to market in the prototype is made possible from the circuit design, circuit simulation has been used in the circuit design. To improve the analysis of circuit operation and the prediction accuracy of circuit characteristics, it is necessary to improve the accuracy of analysis model for the circuit simulations. Therefore, the source-drain resistance affects the device characteristics according as miniaturization advances, it is necessary to consider a model with good accuracy considering the effect of the source-drain resistance in designing a circuit using a novel device structures. The λ-V_{G} model was proposed in 20 nm gate length MOSFET.[56] This model includes the V_{G} dependence of λ in intrinsic region. However, the effect of source and drain resistance on parameters is not analyzed in detail.

In this chapter, the effects of source and drain resistances on model parameters are researched by circuit simulation using the α power model without the dependence of V_{G} in intrinsic region. In section 3.1, the effects of source and drain resistances are investigated as a function of year and structure. In section 3.2, an effect of source and drain series resistance on the device parameters is investigated. Section 3.3 gives a summary of this chapter.

3.1 The effects of source and drain resistances

Table 3.1 shows the values of device parameters of HP logic technology requirements[57] as a function of year and structure from ITRS 2009. In Table 3.1, L_{g} is the gate length, V_{DD} is the supply voltage, $V_{\mathrm{t,sat}}$ is the saturation threshold voltage for a nominal gate length transistor with drain bias set equal to V_{DD}, $I_{\mathrm{d,sat}}$ is the NMOSFET source current per micron of device width, at 25 $^{\circ}$C, with the drain bias set equal to V_{dd} and with the gate, source, and substrate biases set to zero volt, R_{sd} is the maximum allowable parasitic series source plus drain resistance (i.e., total resistance for the two sides) per micron of MOSFET width.

According to this prediction, the size of the MOSFET, the gate length especially is steadily reduced, it reaches down to 20 nm or less in 2013. Parameter values can be roughly sorted by the structure of the three types. The planar bulk as a conventional MOSFET, UTB FD SOI as a SOI MOSFET, and MG is used as a generic DG MOSFET and FinFET. The effects of R_{S} and R_{D} can be investigated using the equivalent circuit in Fig. 2.1. Source resistance R_{S} and drain resistance R_{D} is connected an intrinsic part and the external terminal applied V_{DS} and V_{GS}. When the internal voltages in an intrinsic part of MOSFET are defined as V'_{DS} and V'_{GS}, the following equations are obtained.

$$V'_{\mathrm{DS}} = V_{\mathrm{DS}} - I_{\mathrm{D}} \cdot (R_{\mathrm{S}} + R_{\mathrm{D}}), \tag{3.1}$$

$$V'_{\mathrm{GS}} = V_{\mathrm{GS}} - I_{\mathrm{D}} \cdot R_{\mathrm{S}}, \tag{3.2}$$

$$R_{\mathrm{SD}} = R_{\mathrm{S}} + R_{\mathrm{D}}. \tag{3.3}$$

The drain current I_{D} is a function of the voltage V'_{GS} and V'_{DS} in the intrinsic part. The circuit characteristics are determined by the saturation drain current. The saturation current is characterized by overdrive voltage ($V_{\mathrm{GS}} - V_{\mathrm{TH}}$). In order to investigate the effects of R_{S} and R_{D} on circuit characteristics, the ratio of the overdrive voltage to the supply voltage is calculated by Eq. (3.4).

$$\frac{V'_{\mathrm{GS}} - V_{\mathrm{TH}}}{V_{\mathrm{DD}}} \tag{3.4}$$

The ratios of the overdrive voltage to the supply voltage are shown in Fig. 3.1 as a function of the structure according to Table 3.1. In the case of the calculation, we used the following equations as a channel width W of the MOSFET.

Year	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
L_{g} (nm)	29.0	27.0	24.0	22.0	20.0	18.0	17.0	15.3	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4
V_{DD} (V)	1.00	0.97	0.93	0.90	0.87	0.84	0.81	0.78	0.76	0.73	0.71	0.68	0.66	0.64	0.62	0.60
$V_{\text{t,sat}}$ (mV)																
Planar Bulk	285	289	294	291	295	309	302									
UTBFD-SOI					221	221	220	228	232	236	235					
MG							206	202	207	207	209	219	213	219	228	231
$I_{\text{d,sat}}(\mu\text{A}/\mu\text{m})$																
Planar Bulk	1210	1200	1190	1300	1450	1580	1680									
UTBFD-SOI					1470	1520	1670	1730	1770	1830	1970					
MG							1490	1630	1710	1790	1860	1870	2000	2060	2110	2170
$R_{\text{sd}}(\Omega - \mu\text{m})$																
Planar Bulk	170	170	160	140	130	110	110									
UTBFD-SOI					140	140	130	120	120	120	110					
MG							140	140	130	130	120	120	120	120	110	110

TABLE 3.1: ITRS2009 High-performance logic technology requirements.

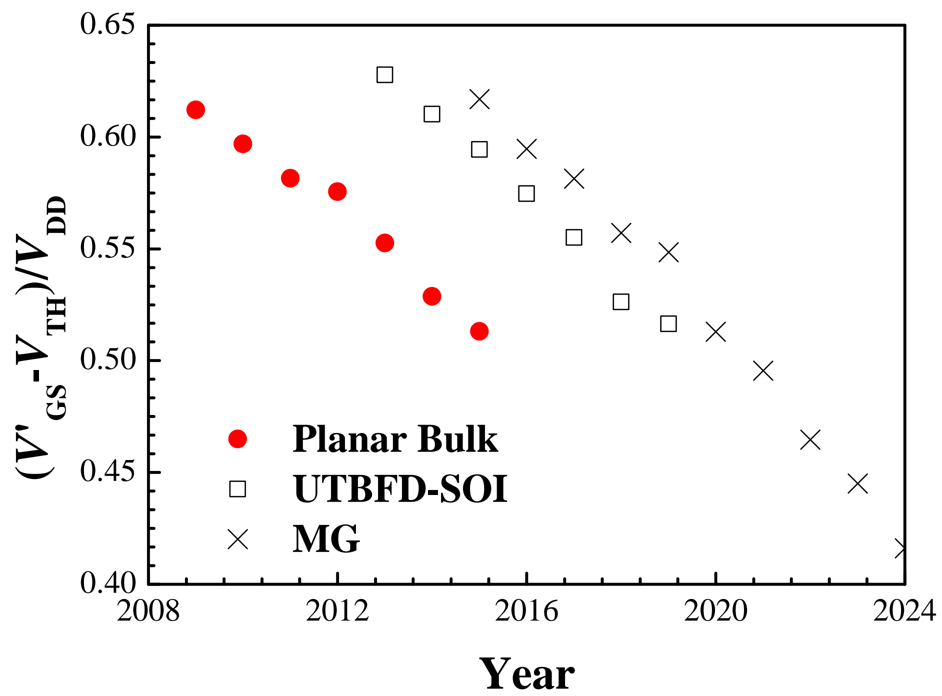


FIGURE 3.1: Current driving capability versus production year for several structures.

$$I_{\mathrm{D}} = I_{\mathrm{d,sat}} \cdot W. \tag{3.5}$$

$$R_{\mathrm{SD}} = \frac{R_{\mathrm{sd}}}{W}. \tag{3.6}$$

$$V_{\mathrm{TH}} = T_{\mathrm{t,sat}}. \tag{3.7}$$

$$V_{\mathrm{GS}} = V_{\mathrm{DD}}. \tag{3.8}$$

In Eqs. (3.5)-(3.8), $I_{\mathrm{d,sat}}$ is the saturation current per micron of device width, R_{sd} is the parasitic series source plus drain resistance per micron of MOSFET width, $V_{\mathrm{t,sat}}$ is the saturation threshold voltage for a nominal gate length transistor with drain bias set equal to V_{DD}. It is assumed that drain resistance R_{D} and the source resistance R_{S} are equal. V'_{GS} is included the effect of R_{S} because of the use of Eq. (3.2).

In Fig. 3.1, we found that the ratio of the overdrive voltage decreases as the production year pass in any structure. The ratio of the planar bulk is 61.2% in 2009 drops to 51.3% in 2015. Characteristics recover temporarily by changing the structure, the ratio of UTB FD-SOI and MG are 59.4 and 61.7% in 2015, respectively. However, the ratios of UTB FD-SOI and MG are down 51.6 and 41.6% in 2019 and 2024 even the structure of these, respectively.

The threshold voltage is changed as the structure and production year change. Therefore, the ratios of the overdrive voltage are also included the varying effect of V_{TH} not only the effect of the source-drain resistance. To investigate the effect only of the source-drain resistance, the following equation excluded the effect of the threshold V_{TH},

$$\frac{V'_{\mathrm{GS}} - V_{\mathrm{TH}}}{V_{\mathrm{GS}} - V_{\mathrm{TH}}}, \tag{3.9}$$

is calculated. In Eq. (3.9), V'_{GS} is the intrinsic gate voltage, V_{GS} is the applied gate voltage. The results are shown in Fig. 3.2.

In Fig. 3.2, the ratios remain constant at about 85% until 2012 in planar bulk, but then begin to fall from 2013, to 81.8% in 2015. The ratio drops every year both UTBFD-SOI and MG, first one is down from 84.1% in 2013 to 77.2% in 2019 and the other one is down from 82.7% in 2015 to 67.7% in 2024, respectively. Moreover, the characteristic continues to become worse as the structure changes, the properties are not recovered, the effect of R_{S} becomes important in any given year. From the above, the effect of the source-drain resistance due to the difference of the structure is small, and we found that the effect increases as the miniaturization progresses.

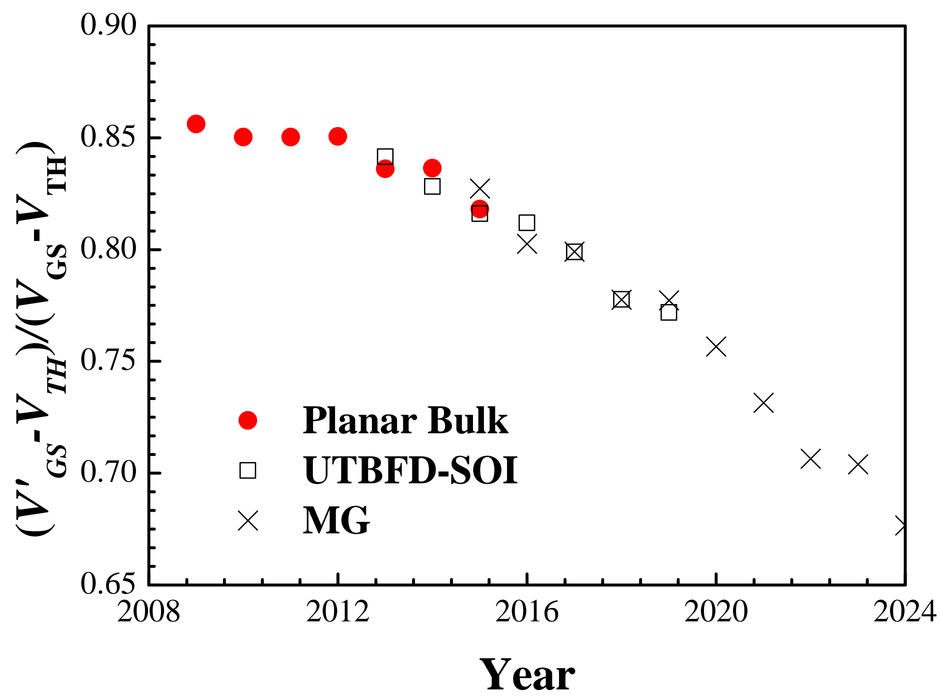


FIGURE 3.2: Current driving capability without effects of V_{TH} versus production year for several structures.

3.2 The effects of R_S and R_D on MOSFET characteristics

In a 20 nm gate length MOSFET, we investigated the impact of the source-drain resistance on the characteristics of the MOSFET. The α power model[58] is used as MOSFET model analysis of the intrinsic part. The saturation drain current of the α power model is simply expressed from Eqs. (2.48) and (2.49) as follows[59]

$$I_\mathrm{D} = I_\mathrm{DSAT0}(1 + \lambda_0 V'_\mathrm{DS}), \tag{3.10}$$

$$I_\mathrm{DSAT0} = \frac{W}{L} B (V'_\mathrm{GS} - V_\mathrm{TH})^\alpha. \tag{3.11}$$

The saturation current I_DSAT0 does not include the effect of the source and drain resistance. In Eqs. (3.10) and (3.11), L is the gate length, W is the gate width, λ_0 is channel length modulation (without the effect of R_S and R_D), and, B and α are the parameters related to the saturation region. The model parameters are used the extracted measured values[54] from the I_D-V_D characteristics of 20 nm nMOSFET[56]. The extracted parameters are shown in Table 3.2.

The model equations are incorporated into a circuit simulator, and the drain current is determined by the circuit simulation of the equivalent circuit in Fig. 2.1. According to the determined drain current, we analyzed the model parameter λ and I_DSAT including the effect of the source and drain resistance. The model equation is used as

$$I_\mathrm{D} = I_\mathrm{DSAT}(R_\mathrm{S}, R_\mathrm{D})(1 + \lambda(R_\mathrm{S}, R_\mathrm{D})V_\mathrm{DS}), \tag{3.12}$$

where, $I_\mathrm{DSAT}(R_\mathrm{S}, R_\mathrm{D})$ and $\lambda(R_\mathrm{S}, R_\mathrm{D})$ are the saturation current and the channel length modulation including the effect of the source and drain resistance, after this, these are described as I_DSAT and λ. We analyzed R_S and R_D varies from 0 to 100 Ω. α is known to enter the region of 0.8 - 1.1 from 2 as the gate length is miniaturized. To investigate the gate voltage dependence of the effects of the source and drain resistance on the parameters I_DSAT and λ, α is assumed 2 for the long channel MOSFET and 1 for the short channel MOSFET. The other parameters except α are same as in Table 3.2.

When $\alpha = 2$ and $R_\mathrm{D} = 0\ \Omega$, the channel length modulations determined from the analysis results as R_S changes are shown in Fig. 3.3. To investigate the dependence of α, λ is analyzed in the same manner as $\alpha = 1$. The results are shown in Fig. 3.4.

In Fig. 3.3, when $R_\mathrm{S} = 10\ \Omega$, λ is 0.8897 and 0.8712 at $V_\mathrm{GS} = 0.6$ V and $V_\mathrm{GS} = 1.0$ V, and when $R_\mathrm{S} = 100\ \Omega$, λ is 0.8374 and 0.7136 at $V_\mathrm{GS} = 0.6$ V and $V_\mathrm{GS} = 1.0$ V, respectively.

Parameter	Value
L(m)	2×10^{-8}
W(m)	1×10^{-6}
B	1.469×10^{-5}
α	0.8885
λ_0(1/V)	0.8961
V_{TH}(V)	0.4267

Table 3.2: Extracted model parameters.

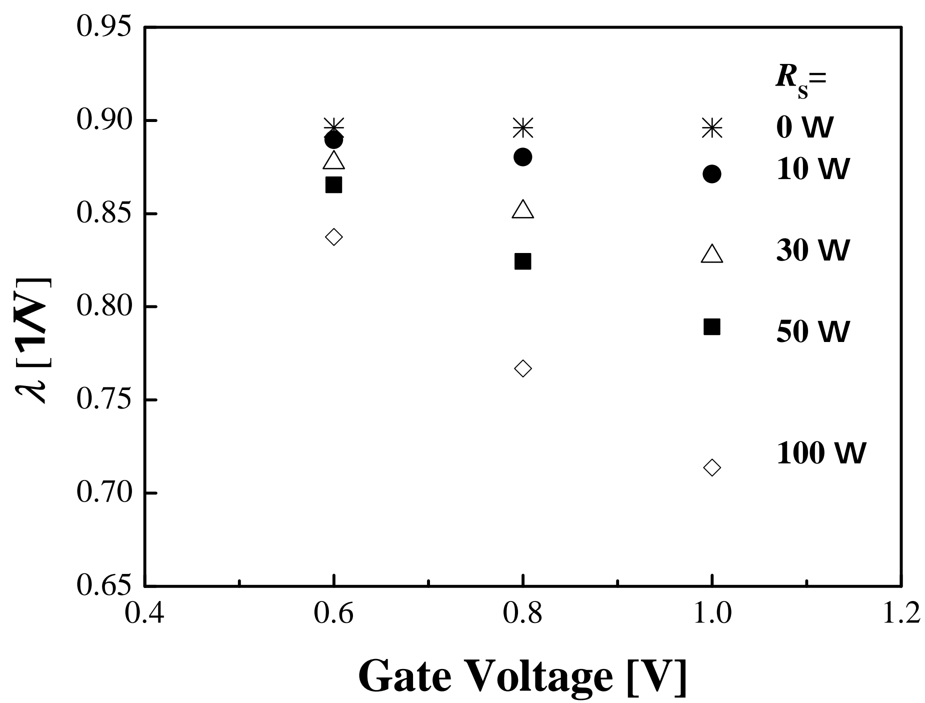


FIGURE 3.3: Channel length modulation coefficient λ versus gate voltage for long channel devices ($\alpha = 2$).

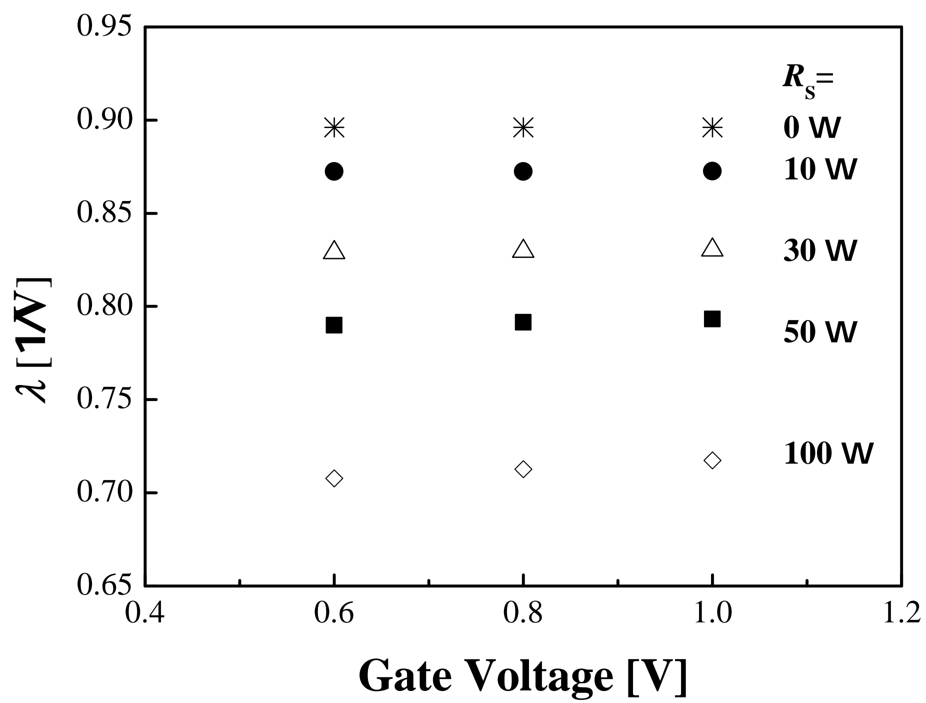


Figure 3.4: Channel length modulation coefficient λ versus gate voltage for long channel devices ($\alpha = 1$).

In Fig. 3.4, when $R_{\rm S} = 10\ \Omega$, λ is 0.8724 and 0.8725 at $V_{\rm GS} = 0.6$ V and $V_{\rm GS} = 1.0$ V, and when $R_{\rm S} = 100\ \Omega$, λ is 0.7078 and 0.7173 at $V_{\rm GS} = 0.6$ V and $V_{\rm GS} = 1.0$ V, respectively. The differences of ($V_{\rm GS} = 0.6$) and ($V_{\rm GS} = 1.0$) are calculated by following equation.

$$\Delta\lambda = \frac{|\lambda(V_{\rm GS} = 1.0) - \lambda(V_{\rm GS} = 0.6)|}{\lambda(V_{\rm GS} = 0.6)} \tag{3.13}$$

The $R_{\rm S}$ dependence of equation (3.13) shows in Fig. 3.5.

In Fig. 3.5, when $\alpha = 2$, as $R_{\rm S}$ increases, the difference of λ increases too, and the difference of that is 15% at $R_{\rm S} = 100\ \Omega$. However, when $\alpha = 1$, the ratio of the difference is 1.4% at $R_{\rm S} = 100\ \Omega$ even if $R_{\rm S}$ increase. In other words, there is no gate voltage dependence when $\alpha = 1$. Therefore, the influence of the source-drain resistance on the channel length modulation becomes independent of the gate voltage as the gate length shrinks.

Then, we calculate the relative error $\Delta I_{\rm DSAT}$ of $I_{\rm DSAT}$ by the following equation.

$$\Delta I_{\rm DSAT} = \frac{|I_{\rm DSAT}(R_{\rm S}) - I_{\rm DSAT}(R_{\rm S} = 0)|}{I_{\rm DSAT}(R_{\rm S} = 0)} \tag{3.14}$$

The results $\Delta I_{\rm DSAT}$ are shown as α is 2 and 1 in Figs. 3.6 and 3.7, respectively. $\Delta I_{\rm DSAT}$ is found to change to a linear function in both cases $\alpha = 2$ and $\alpha = 1$. Therefore, the influence of the source-drain resistance on the saturation drain current of is the unchanged linear function as the gate length decreases.

3.3 Summary

The importance of source-drain resistance was tested for effect on the characteristics of the MOSFET to become increasingly important in the design and development of new device structures in the future. We calculated the ratio of the overdrive voltage to the supply voltage as a function of the MOSFET structure. The change of that due to the structure change is small, we found that the effect of the source-drain resistance becomes larger every year. The effects of the source and drain series resistance on the MOSFET characteristics were investigated using circuit simulation. As a result, the influence of the source and drain series resistance on the channel length modulation was found to be independent of the gate voltage the gate length is reduced.

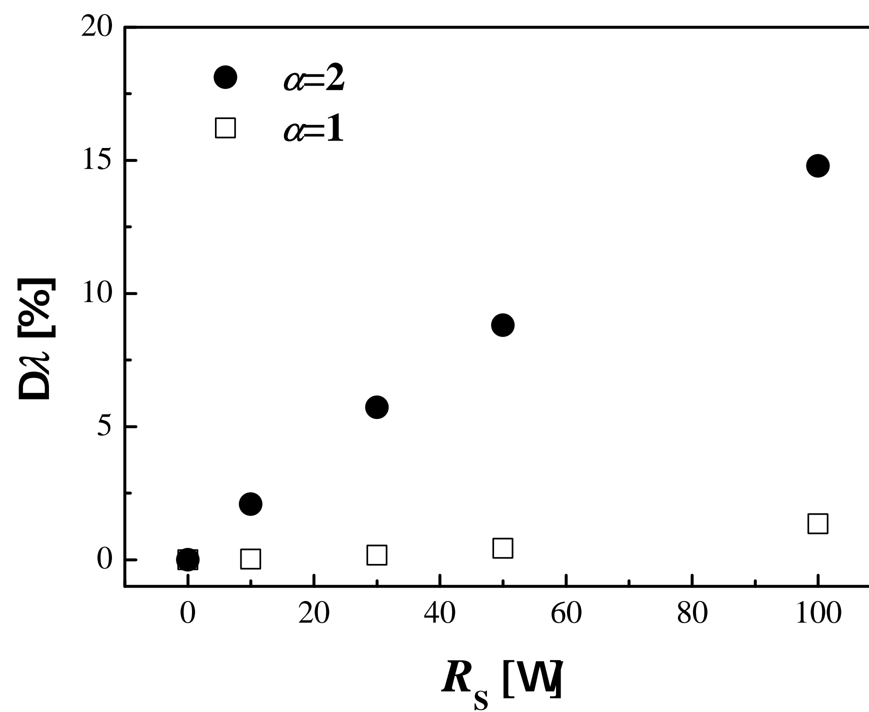


FIGURE 3.5: Relative difference of channel length modulation coefficient λ versus source and drain resistance for long and short channel devices.

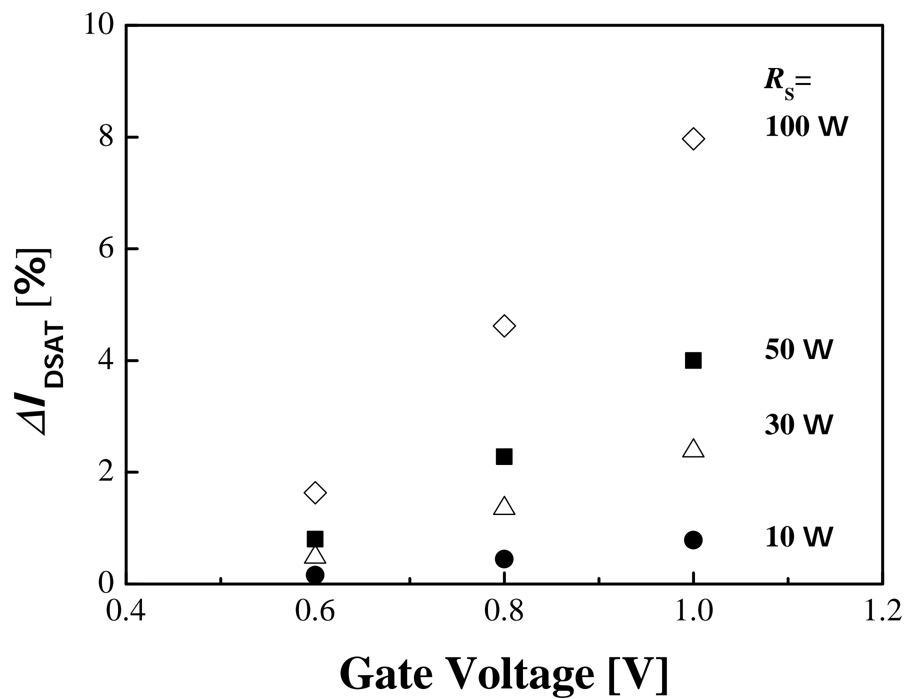


FIGURE 3.6: Relative difference of I_{DSAT} versus gate voltage for long channel devices ($\alpha = 2$).

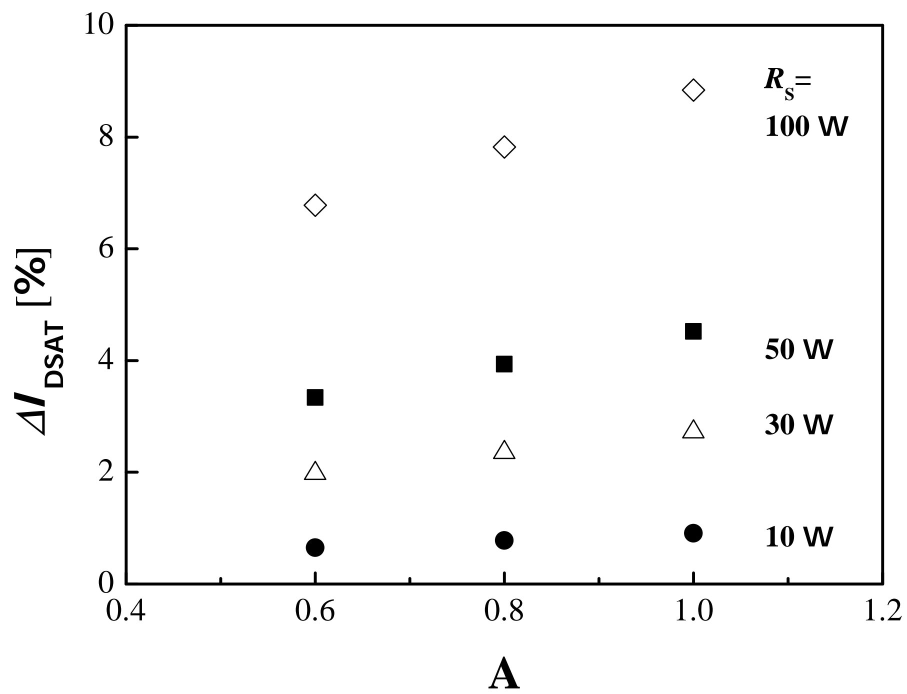


FIGURE 3.7: Relative difference of I_{DSAT} versus gate voltage for long channel devices ($\alpha = 1$).

Chapter 4

Higher-Order Effect of Source-Drain Series Resistance on Saturation Drain Current in Sub-20 nm MOSFETs

In the traditional planar bulk MOSFETs, extended source and drain regions with shallow junction and higher doping concentrations have been used to prevent not only the short-channel effects but also the increase of the sheet resistance.[34] The extended source and drain series resistance was modeled in an early study of Kim *et al.*[60, 61] Low series resistance is required for CMOS technology to keep up with downscaling.[62–64] In device design and development for advanced MOSFETs, drain current reduction due to the series resistance becomes a critical issue as CMOS technologies are scaled deeper into the nanoscale regime.[27, 65–67] The series resistance has been important issues for modeling I-V characteristics of the extremely scaled MOSFETs. Many works [54, 68–74] have modeled the effects of the series resistance on I-V characteristics. Analytical current models are approximated using the Taylor expansion of the series resistance. The models have been researched and analyzed at the saturated current region in the works. However, higher order effects of the series resistance are not mentioned in detail.

In this chapter, we investigate a reduction in saturation drain current by the source and drain series resistance in the sub-20 nm technology node. We describe model parameters of sub-20 nm MOSFETs and simulation methods. The reduction rate of the saturation drain current owing to the effect of the series resistance is calculated by using the derived analytical current model in section 2.2. An effect of higher-order terms of

the saturation drain current and the relationships between physical parameters and the current reduction are discussed.

4.1 Simulation

To investigate the saturation drain current including the effect of the series resistance, the reduction rate of I_{Dsat} is calculated as a function of the gate length. The reduction rate of I_{Dsat} is defined as follows:

$$\frac{|I_{\text{Dsat}} - I_{\text{Dsat0}}|}{I_{\text{Dsat0}}}, \tag{4.1}$$

where I_{Dsat0} is the saturation drain current without the effect of the series resistance calculated using Eq. (2.6) and the saturation drain current including the resistance effect I_{Dsat} is calculated using Eq. (2.34). Values of the parameters used in the simulated devices are shown in Table 4.1.

L_{g} and V_{dd} are chosen from the ITRS 2007.[23] ITRS publishes annual reports focusing on various technologies, such as HP technology, LSTP technology, and LOP technology in the logical device technology. The supply voltages are 1.1, 1.0, and 0.8 V in HP, LSTP, and LOP technologies, respectively. In the LOP technology, the focus is on reducing operating power dissipation. To effectively reduce the power dissipation, the supply voltage is minimized. By decreasing the supply voltage, an increase in spreading resistance is induced.[29] The LOP technology is chosen in this simulation according to the minimum supply voltage. The source resistance per unit gate width is calculated under the assumption that R_{S} is one-half of R_{SD}. V_{gt} is given by

$$V_{\text{gt}} = V_{\text{dd}} - V_{\text{th,on}}, \tag{4.2}$$

$$V_{\text{th,on}} = V_{\text{t,sat}} + 0.03, \tag{4.3}$$

where $V_{\text{th,on}}$ is the saturated threshold voltage used for on-state current calculation. $V_{\text{th,on}}$ is modified by adding 0.03 V to a saturated threshold voltage $V_{\text{t,sat}}$.[49] The saturated threshold voltage $V_{\text{t,sat}}$ is used for the extrapolation of channel leakage current for $V_{\text{GS}} = 0$ and $V_{\text{DS}} = V_{\text{dd}}$. L_{el}, μ_{eff}, E_{c}, and d are calculated by using the MASTAR[49] results. The model for the assessment of CMOS technologies and roadmaps (MASTAR) is an analytical model used in ITRS. C_{ox} is identical to the electronic gate-oxide capacitance $C_{\text{ox_elec}}$ in the result of the MASTAR.

TABLE 4.1: Values of the parameters used in the simulated devices.

L_{g}	(nm)	32	28	25	22	20	18
L_{el}	(nm)	21.6	19.2	17.5	16.4	15.1	13.4
R_{S}	$(\Omega \cdot \mu\mathrm{m})$	95	95	95	95	95	95
C_{ox}	$(\mathrm{fF}/\mu\mathrm{m})$	18.8	23.9	25.9	27.9	30.6	30.8
μ_{eff}	$(\mathrm{cm^2V^{-1}s^{-1}})$	491	581	557	607	585	582
E_{c}	(MV/cm)	4.48	3.79	3.94	3.62	3.76	3.78
V_{dd}	(V)	0.8	0.8	0.8	0.7	0.7	0.7
$V_{\mathrm{th,on}}$	(V)	0.294	0.296	0.289	0.259	0.246	0.249
V_{gt}	(V)	0.506	0.504	0.511	0.441	0.454	0.456
d		0.334	0.245	0.241	0.224	0.217	0.242

4.2 Results

Figure 4.1 shows the results of I_{Dsat0} and I_{Dsat} calculated using Eqs. (2.6) and (2.34) as a function of the gate length, respectively. Differences between I_{Dsat0} and I_{Dsat} increase from 131 to 332 μA/μm as the gate length decreases from 32 to 18 nm. As the gate length decreases, both saturation drain currents increase except for the 22 nm MOSFET. The drain current of the 22 nm MOSFET decreases since the supply voltage changes from 0.8 to 0.7 V.

Figure 4.2 shows the reduction rate of I_{Dsat} described by Eq. (4.1) as a function of the gate length. The reduction rate increases from 15.8 to 24.0% as the gate length decreases from 32 to 18 nm. As the gate length decreases from 32 to 28 nm, the reduction rate increases from 15.8 to 19.6%. The largest gap of the rates between generations is between 32 and 28 nm generations. For 18 and 20 nm MOSFETs, the rates are 24.0 and 23.8%, respectively. The rates are almost constant below 20 nm. The gate voltage drop depends on I_{Dsat} and R_{S}, as shown by eq. (2.32). R_{S} is 95 $\Omega \cdot \mu$m in the 18 - 32 nm gate length range. Thus, the gate voltage drop and the reduction rate depend on I_{Dsat}. The reduction rate should also decrease for the 22 nm MOSFET. By comparing Fig. 4.1 with Fig. 4.2, the current drop does not depend on only I_{Dsat} and R_{S}.

To investigate the effect of higher-order terms, we calculated the absolute Nth-order terms using eqs. (2.44)-(2.47). The results of the Nth-order term are shown in Table 4.2 as a function of the gate length. The 1st- and 3rd-order terms have negative values. Using Table 4.2, we calculated the ratio of the Nth-order term to the sum of all absolute order terms. The ratio is defined as

$$\frac{|a_{\mathrm{N}} R_{\mathrm{S}}^{\mathrm{N}}|}{\sum_{i=1}^{4} |a_{\mathrm{i}} R_{\mathrm{S}}^{\mathrm{i}}|}. \tag{4.4}$$

Figure 4.3 shows results of the component ratio as a function of the gate length. The component ratios of 1st-order terms decrease from 80.7 to 68.6% as the gate length decreases from 32 to 18 nm. The component ratios of 2nd-order terms increase from 15.6 to 22.0% as the gate length decreases. The component ratios of 3rd-order terms increase from 3.0 to 7.1% as the gate length decreases. In particular, for 2nd-order terms, the component ratios are over 20% for 22 nm and below MOSFETs. As the gate length decreases, any effect of higher-order terms becomes important for analyzing the effect of the series resistance.

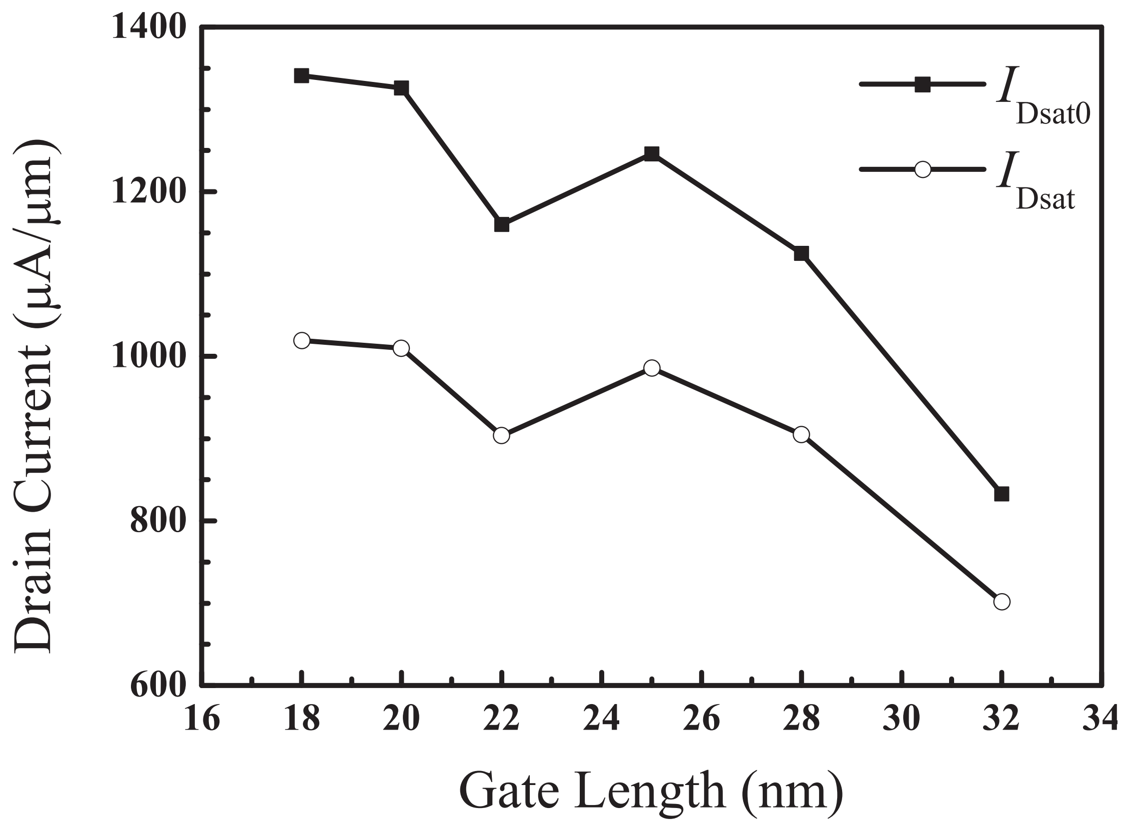


FIGURE 4.1: Saturation drain current without the effect of the series resistance (squares) and saturation drain current including the effect (circles) as a function of the gate length.

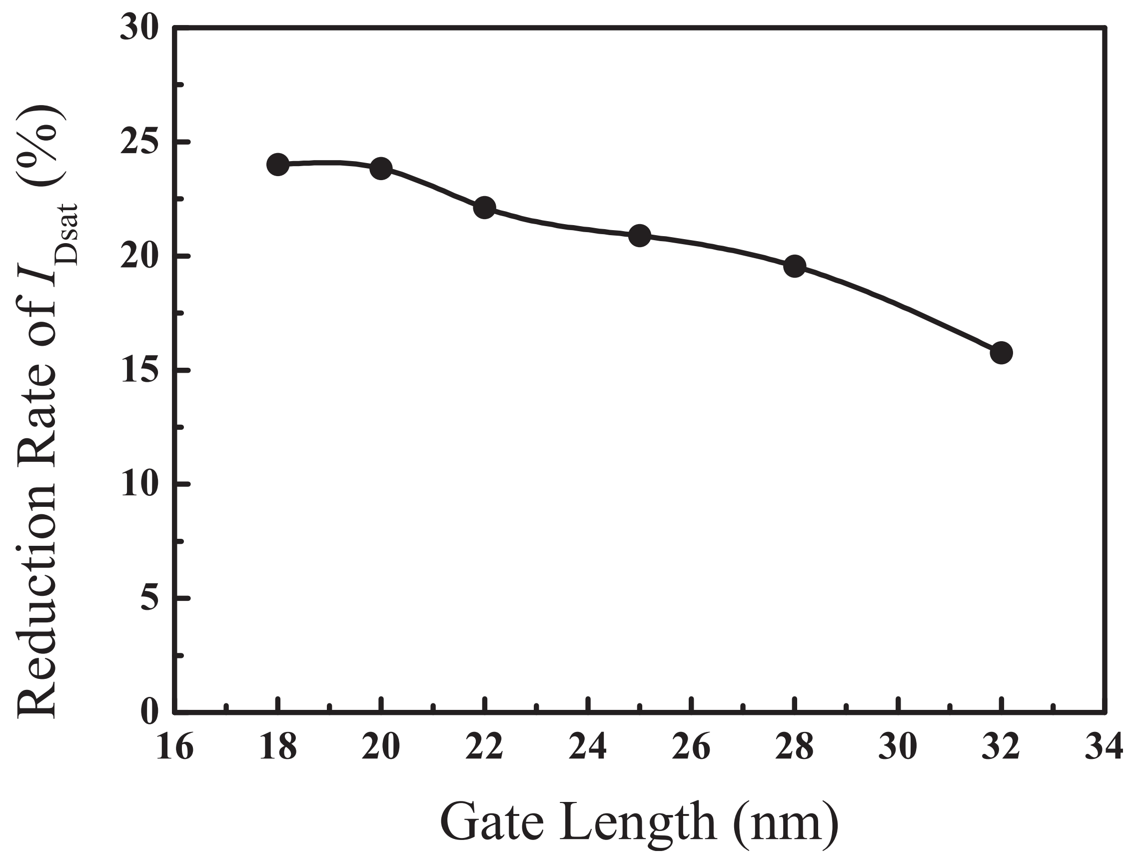


Figure 4.2: Reduction rate by considering source-drain series resistance of I_{Dsat} as a function of the gate length.

TABLE 4.2: Calculated results of absolute Nth-order terms ($a_N R_S^N$).

L_g	(nm)	32	28	25	22	20	18
$a_1 R_S$	($\times 10^{-1}$)	1.88	2.44	2.65	2.85	3.14	3.17
$a_2 R_S^2$	($\times 10^{-2}$)	3.64	6.07	7.14	8.26	10.0	10.2
$a_3 R_S^3$	($\times 10^{-2}$)	0.709	1.51	1.93	2.40	3.20	3.26
$a_4 R_S^4$	($\times 10^{-3}$)	1.39	3.78	5.22	6.99	10.2	10.5

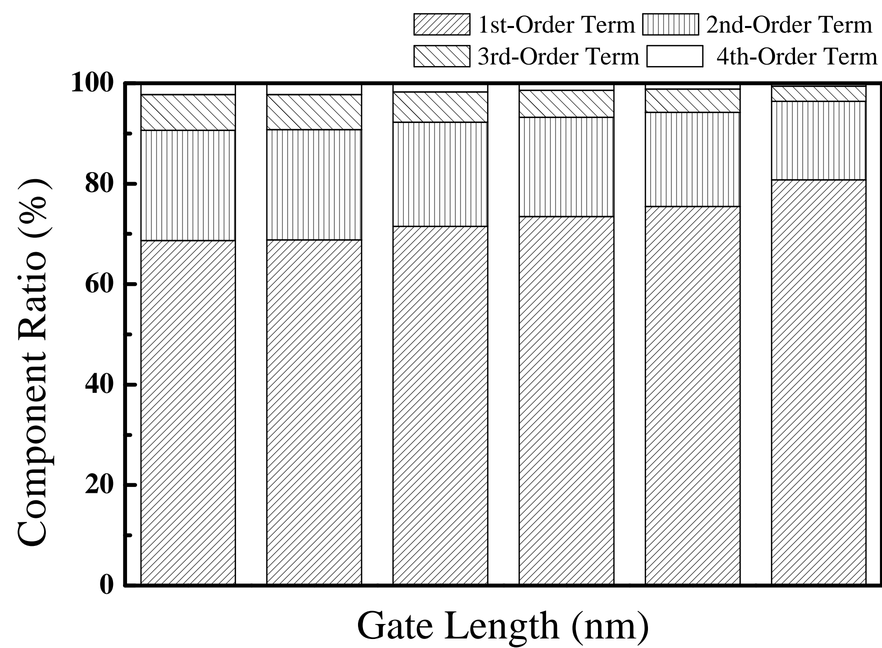


FIGURE 4.3: Component ratio of Nth-order term to the sum of all absolute order terms as a function of the gate length.

4.3 Discussion

To investigate the physical reasons underlying the reduction rate increase, expansion components of the Nth-order term are compared with the reduction rates. Table 4.3 shows the calculated expansion components of the Nth-order terms ($a_{\mathrm{N}} R_{\mathrm{S}}^{\mathrm{N}}$).

Figure 4.4 shows the expansion components of the 1st-order term and the reduction rates as a function of the gate length. The expansion components are normalized by that of the 32 nm MOSFET. The normalized first component increases from 1 to 1.84 as the gate length decreases from 32 to 18 nm. As the gate length decreases from 32 to 28 nm, the first component increases from 1 to 1.35. For 18 and 20 nm MOSFETs, the first components are 1.84 and 1.82, respectively. The first components are almost constant below 20 nm. The increases in first components follows that in reduction rate. The second and third normalized components are about 1 at all gate lengths. There is no dependence on the gate length in the second and third components. The second component is the ratio of the supply voltage to the overdrive voltage. In other words, the supply voltage and the overdrive voltage are well scaled in these gate length regions. Below 32 nm MOSFETs, the first component is a dominant factor in the reduction in I_{Dsat}.

Figure 4.5 shows normalized first components of higher-order terms and the reduction rates as a function of the gate length. The first components increase as the gate length decreases. The increases in first components follow that in reduction rate, as in the case of the 1st-order terms. The second and third components are almost constant as a function of the gate length, as in the case of the 1st-order terms. The difference in first component between 32 and 18 nm increases from 0.84 to 2.39 for the 1st-order and 2nd-order terms such an increase grows as the order increases. As the degree of the order term increases from 1 to 4, the values of the higher-order terms decrease since the unnormalized values of the first components decrease, as shown in Table 4.3.

As shown in Fig. 4.4, the increases in first components follow that in reduction rate. The first component is the ratio of the source resistance to the channel resistance. Since it is assumed that the source resistance is constant in this work, the reduction in saturation drain current is inversely proportional to the channel resistance. The channel resistance is proportional to I_{Dsat0} owing to the fact that the supply voltages are 0.7 and 0.8 V. In Eq. (2.6), I_{Dsat0} is a function of μ_{eff}, C_{ox}, V_{gt}, E_{c}, and L_{el}. The effect of $L_{\mathrm{g}} \cdot E_{\mathrm{c}}$ is insignificant, since $E_{\mathrm{c}} \cdot L_{\mathrm{el}}$ is sufficiently small to ignore. The overdrive voltage drops by 0.05 V below 22 nm MOSFETs. The gate capacitance and the effective mobility are the most effective parameters in the saturation drain current (I_{Dsat0}). As shown in Fig. 4.2, the largest gap of the rates between 32 and 28 nm generations can be explained

TABLE 4.3: Calculated expansion components of Nth-order terms ($a_N R_S^N$).

L_g		(nm)	32	28	25	22	20	18
	First component		0.989	1.34	1.48	1.57	1.80	1.82
$a_1 R_S$	Second component	($\times 10^{-1}$)	1.58	1.59	1.57	1.59	1.54	1.55
	Third component		1.20	1.15	1.14	1.14	1.13	1.12
	First component		0.978	1.78	2.19	2.48	3.24	3.31
$a_2 R_S^2$	Second component	($\times 10^{-2}$)	2.50	2.52	2.45	2.52	2.38	2.40
	Third component		1.49	1.35	1.33	1.32	1.30	1.28
	First component		0.968	2.38	3.24	3.90	5.83	6.03
$a_3 R_S^3$	Second component	($\times 10^{-3}$)	3.95	3.99	3.85	4.00	3.67	3.73
	Third component		1.86	1.59	1.55	1.54	1.50	1.45
	First component		0.957	3.19	4.79	6.14	10.5	11.0
$a_4 R_S^4$	Second component	($\times 10^{-4}$)	6.24	6.33	6.02	6.34	5.66	5.78
	Third component		2.32	1.87	1.81	1.79	1.72	1.66

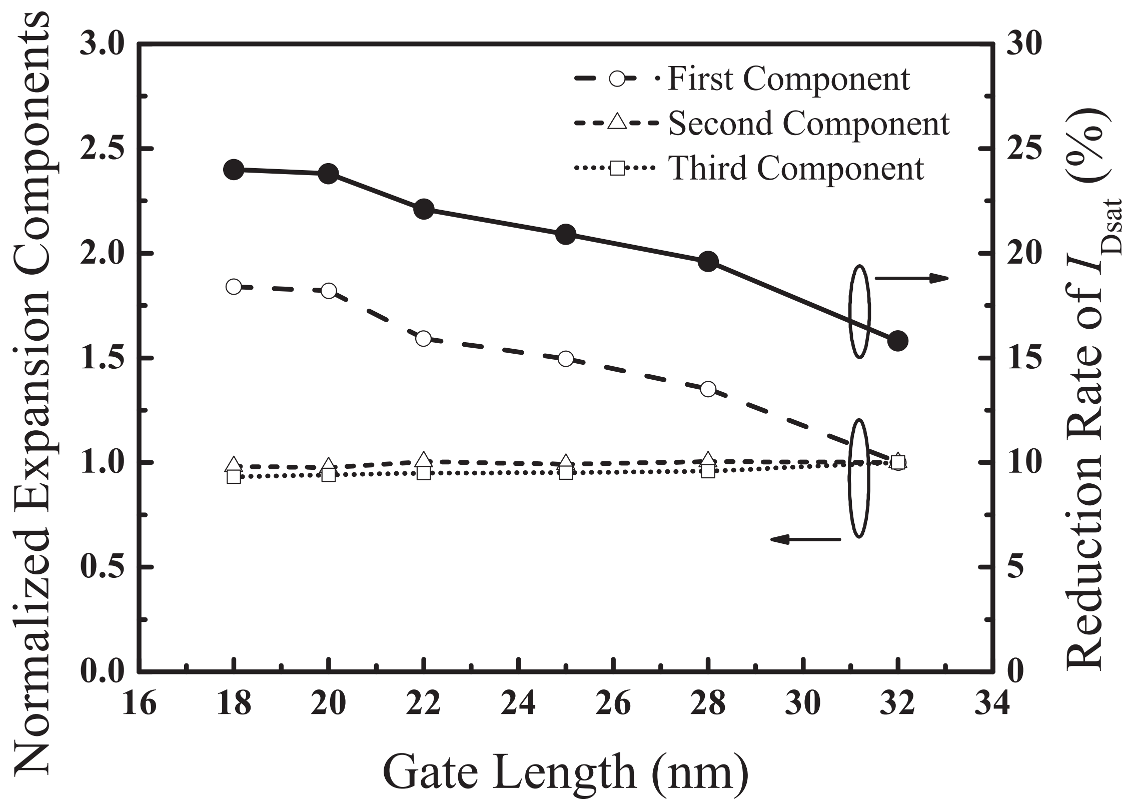


FIGURE 4.4: Normalized expansion components (dashed lines) of 1st-order term and the reduction rates (solid line) of I_{Dsat} as a function of the gate length.

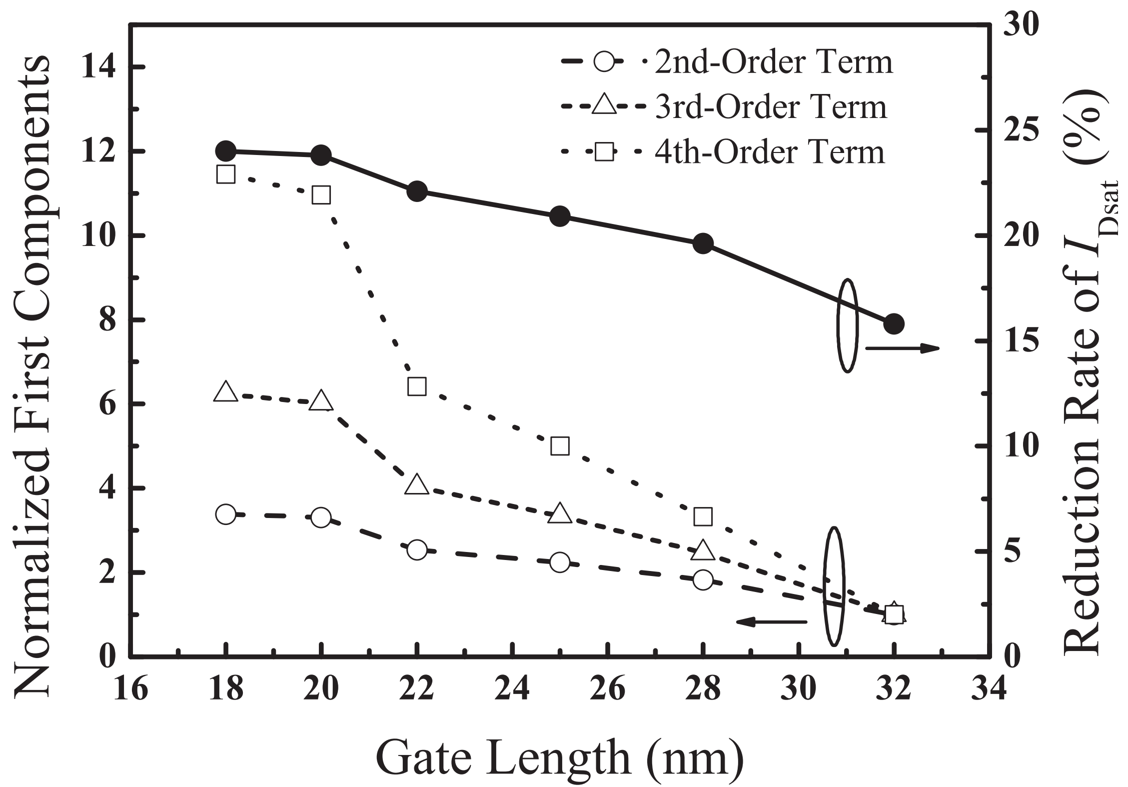


FIGURE 4.5: Normalized first components (dashed lines) of 2nd-order, 3rd-order, and 4th-order terms and the reduction rate (solid line) of I_{Dsat} as a function of the gate length.

by the fact that high-k dielectric materials are available as the gate insulator. Below 20 nm, problems of interface properties and compatibility of the high-k materials limit the decrease in equivalent oxide thickness (EOT) < 0.7 nm.

4.4 Summary

We investigate the saturation drain current reduction by the source and drain series resistance in sub-20 nm MOSFETs. The current reduction is calculated by using the derived analytical current model including the higher-order terms of the series resistance. As a result, the reduction rate increases from 15.8 to 24.0% as the gate length decreases from 32 to 18 nm. The ratios of 1st-order and 2nd-order terms change from 80.7 to 68.6% and from 15.6 to 22.0% as the gate length decreases from 32 to 18 nm, respectively. We find that the higher order terms are important for analyzing the effect of the series resistance as the gate length decreases. From the analysis of the normalized expansion components, the increase in the ratio of the source resistance to the channel resistance leads to that in reduction rate. This implies that the resistance ratio of the source resistance to the channel resistance is a dominant factor in device design and development for sub-20 nm MOSFETs.

Chapter 5

Structural Dependence of Source and Drain Series Resistance on Saturation Drain Current for Sub-20 nm MOSFETs

The continuous scaling has major problems such as SCEs and leakage currents. These problems can be suppressed by structural changes from planer bulk to FD SOI and MG MOSFETs such as tri-gate, gate all around MOSFETs, and FinFET.[75–78] In these advanced MOSFETs, as the fin or channel regions are extremely scaled, tall and narrow extended source and drain regions are formed. The extended regions lead to higher source and drain series resistance.[27, 79, 80] Effects of the series resistance on drain currents increase as supply voltages decrease to reduce the power consumption.[29, 81] Therefore, the effects of the series resistance on drain currents becomes a non-negligible factor in sub-20 nm gate-length regime.[53, 65]

In this chapter, we investigate the structural dependence of source and drain series resistance on the saturation drain current for planner bulk, SOI, and MG MOSFETs in sub-20 nm technology nodes. We describe model simulation methods and parameters of sub-20 nm MOSFETs. A reduction rate of the saturation drain current owing to the effect of the series resistance is calculated in CMOS logic technologies. The reduction rates and expansion components of the saturation current are discussed to clear relationships between physical parameters and the current reduction.

5.1 Simulation

The saturation current including the effect of the series resistance is compared with the current without the effect to investigate the resistance effect on the saturation current for bulk, SOI, and MG MOSFETs. The reduction rate of the saturation current is defined as follows:

$$\frac{|I_{\rm Dsat} - I_{\rm Dsat0}|}{I_{\rm Dsat0}}, \tag{5.1}$$

where $I_{\rm Dsat0}$ is the saturation drain current without the resistance effect calculated using Eq. (2.6) and the saturation drain current including the resistance effect $I_{\rm Dsat}$ is calculated using Eq. (2.38).

Values of the parameters used in the simulated devices are shown in Table 5.1. $L_{\rm g}$ and $V_{\rm dd}$ are chosen from the ITRS 2007.[23] ITRS publishes annual reports focusing on HP, LOP, and LSTP technologies in logical devices. The source resistance per unit gate width is calculated under the assumption that $R_{\rm S}$ is one-half of $R_{\rm SD}$. $V_{\rm gt}$ is given by

$$V_{\rm gt} = V_{\rm dd} - V_{\rm th,on}, \tag{5.2}$$

$$V_{\rm th,on} = V_{\rm t,sat} + \Delta V, \tag{5.3}$$

where $V_{\rm th,on}$ is the saturated threshold voltage used for on-state current calculation. $V_{\rm th,on}$ is modified by adding a modified model parameter ΔV to a saturated threshold voltage $V_{\rm t,sat}$.[49] ΔV is assumed to be 0.03 V. The saturated threshold voltage $V_{\rm t,sat}$ is used for the extrapolation of channel leakage current at $V_{\rm GS} = 0$ and $V_{\rm DS} = V_{\rm dd}$. EOT is the equivalent oxide thickness. $K_{\rm bal}$ means the effective ballistic enhancement factor in ITRS. $L_{\rm el}$, $\mu_{\rm eff}$, $E_{\rm c}$, d, and EOT are calculated by using the results of the model for the assessment of CMOS technologies and roadmaps (MASTAR)[49]. It is an analytical model used in ITRS. $C_{\rm ox}$ is identical to the electronic gate-oxide capacitance $C_{\rm ox_elec}$ in the result of the MASTAR. In the MASTAR, the source and drain resistances $R_{\rm SD}$ were used as the source resistance. However, one-half of the source and drain resistances is used as the source resistance in this work. The reduction rates of the saturation current are calculated for bulk, SOI, and MG MOSFETs in HP, LOP, and LSTP technologies.

A key transistor performance of the requirements is the intrinsic switching frequency ($1/\tau = I/CV$) for device scaling in the ITRS reports. Scaling targets of this parameter are 13 - 17% improvement per year. In HP technology, to scale the device with the improvement, the scaling of the gate oxide thickness is important. However, the gate leakage current due to direct tunneling increases exponentially as the gate oxide thickness decreases below 1.2 nm. Therefore, the gate leakage current density is a critical issue. EOT is set as thin as possible with the tolerable gate leakage current density. As the

TABLE 5.1: Values of the parameters used for HP, LOP, and LSTP technologies in the simulated devices.

		High Performance			Low Operating Power			Low STandby Power		
		Bulk	SOI	MG	Bulk	SOI	MG	Bulk	SOI	MG
L_{g}	(nm)	16	16	16	20	20	20	22	22	22
L_{el}	(nm)	12.4	12.4	8.5	15.0	15.0	11.2	17.5	17.2	12.4
EOT	(nm)	0.55	0.60	0.80	0.80	0.90	0.90	1.20	1.30	1.40
V_{dd}	(V)	0.95	1.00	1.00	0.70	0.70	0.70	1.00	0.90	0.85
$V_{\mathrm{th,on}}$	(mV)	131	119	145	276	248	237	582	425	410
E_{c}	(MV/cm)	8.31	6.72	5.29	3.76	3.32	3.17	5.57	3.48	3.37
R_{S}	($\Omega \cdot \mu$m)	90	90	90	95	95	95	90	100	105
C_{ox}	(fF/μm)	42.0	34.5	28.8	30.5	26.5	26.5	22.9	20.3	19.2
μ_{eff}	(cm^{2}V^{-1}s^{-1})	265	327	416	585	663	656	395	574	594
d		0.190	0.015	0.000	0.217	0.019	0.000	0.343	0.025	0.000
V_{gt}	(mV)	819	881	855	424	452	463	418	475	440
K_{bal}		1.00	1.10	1.17	1.00	1.00	1.00	1.00	1.00	1.00
Switching Speed	(GHz)	2326	2778	2941	1333	1449	1449	806	980	980

structure of MOSFETs changes the planner bulk to the SOI or MG MOSFETs, the requirement of EOT increases from 0.55 nm at the planner bulk to 0.60 nm at the SOI or 0.80 nm at the MG MOSFETs because the gate electrodes are performed more than one side. To compensate this loss, the carrier mobilities in channel regions increase 265, 327, 416 $cm^2V^{-1}s^{-1}$ for the bulk, SOI and MG MOSFETs as the structure changes, respectively.In LOP technology, to scale the device with the low operating power, the lowering of the supply voltage is the most effective way to decrease the dynamic power consumption. In order to keep the reasonable saturation current with the lowest supply voltage (= 0.7 V), the threshold voltage has to be reduced as small as possible. The threshold voltage is reduced by the more effective gate control as the structure of MOSFET changes. This merit enhances the overdrive voltage. The overdrive voltages increase from 424 mV at the planner bulk to 452 mV at the SOI or 463 mV at the MG MOSFETs. In LSTP technology, to scale the device with the low standby power, the suppression of the off-state leakage current is important. To achievement the low leakage current needs to increase the threshold voltage. It follows the supply voltage to guarantee the reasonable overdrive voltage. However, the thickest EOT (1.2 - 1.4 nm) influenced by the smallest requirement of the gate leakage current density get worth the device performance. As the structure changes, this demerit can be suppressed by the improvement of the carrier mobility in the channel region.

5.2 Results

Table 5.2 shows the calculated saturation currents and the reduction rates of the current for bulk, SOI, and MG MOSFETs in HP, LOP, and LSTP technologies.

Figure 5.1 shows the reduction rates of the saturation current influenced by the series resistance for bulk, SOI, and MG MOSFETs in HP, LOP, and LSTP technologies. In HP technology, the reduction rates are 29.0, 25.3, and 22.1% for bulk, SOI, and MG MOSFETs, respectively. In LOP technology, the reduction rates are 23.8, 21.5 and 20.7% for bulk, SOI, and MG MOSFETs, respectively. In LSTP technology, the reduction rates are 17.5, 16.7, and 16.6% for bulk, SOI, and MG MOSFETs, respectively. The reduction rate decreases in all technologies as the structure of MOSFETs is advanced.

Differences of the reduction rates compared with each structure are different for each technology. Figure 5.2 shows difference of the reduction rates between each structure in HP, LOP, and LSTP technologies. The differences of the reduction rates between bulk-SOI, bulk-MG, and SOI-MG are 3.7, 6.9, and 3.2% in HP technology, respectively. The differences of the reduction rates between bulk-SOI, bulk-MG, and SOI-MG are 2.3, 3.1, and 0.8% in LOP technology, respectively. The differences of the reduction rates

TABLE 5.2: Calculated results of the reduction rate on saturation current by the series resistance.

		High Performance			Low Operating Power			Low STandby Power		
		Bulk	SOI	MG	Bulk	SOI	MG	Bulk	SOI	MG
I_{Dsat0}	(μA/μm)	3297	3356	3007	1226	1185	1187	800	854	770
I_{Dsat}	(μA/μm)	2342	2508	2343	935	931	942	660	711	642
Reduction rate	(%)	29.0	25.3	22.1	23.8	21.5	20.7	17.5	16.7	16.6

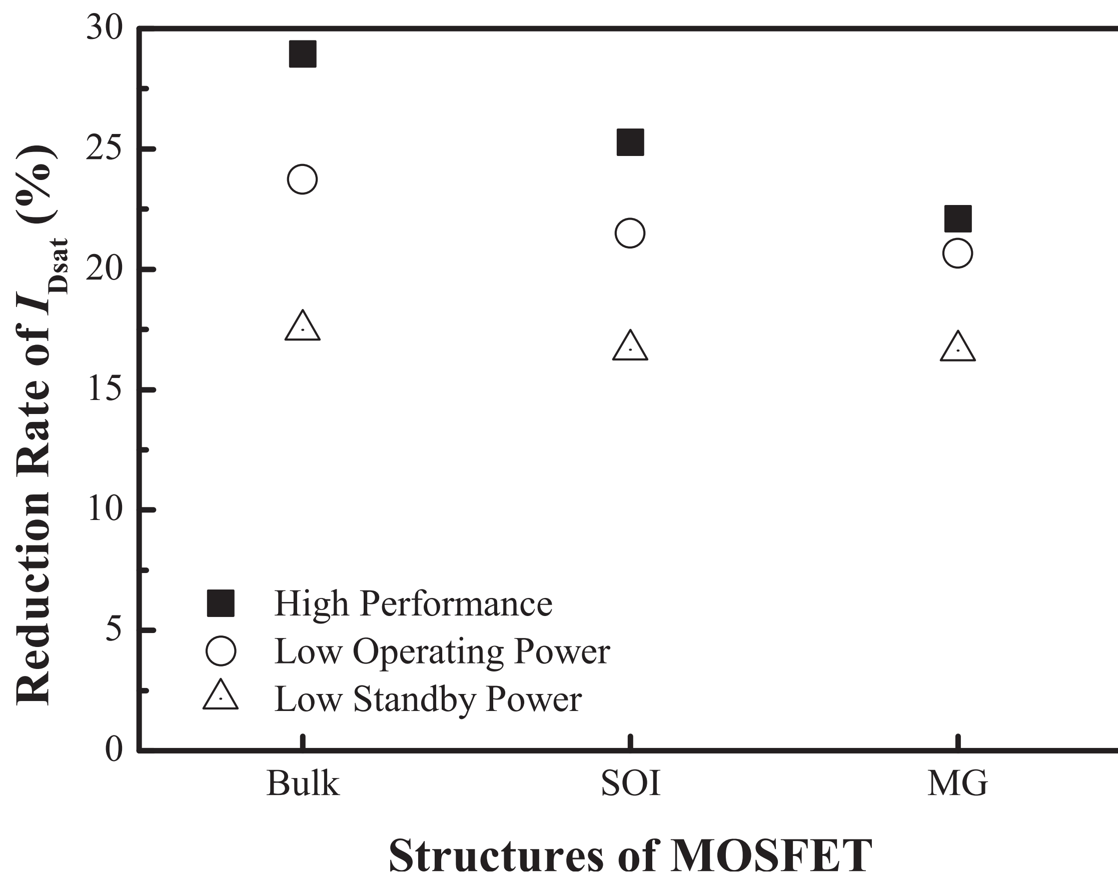


FIGURE 5.1: Reduction rate of the saturation current influenced by the series resistance for bulk, SOI, and MG structure in HP, LOP, and LSTP technologies.

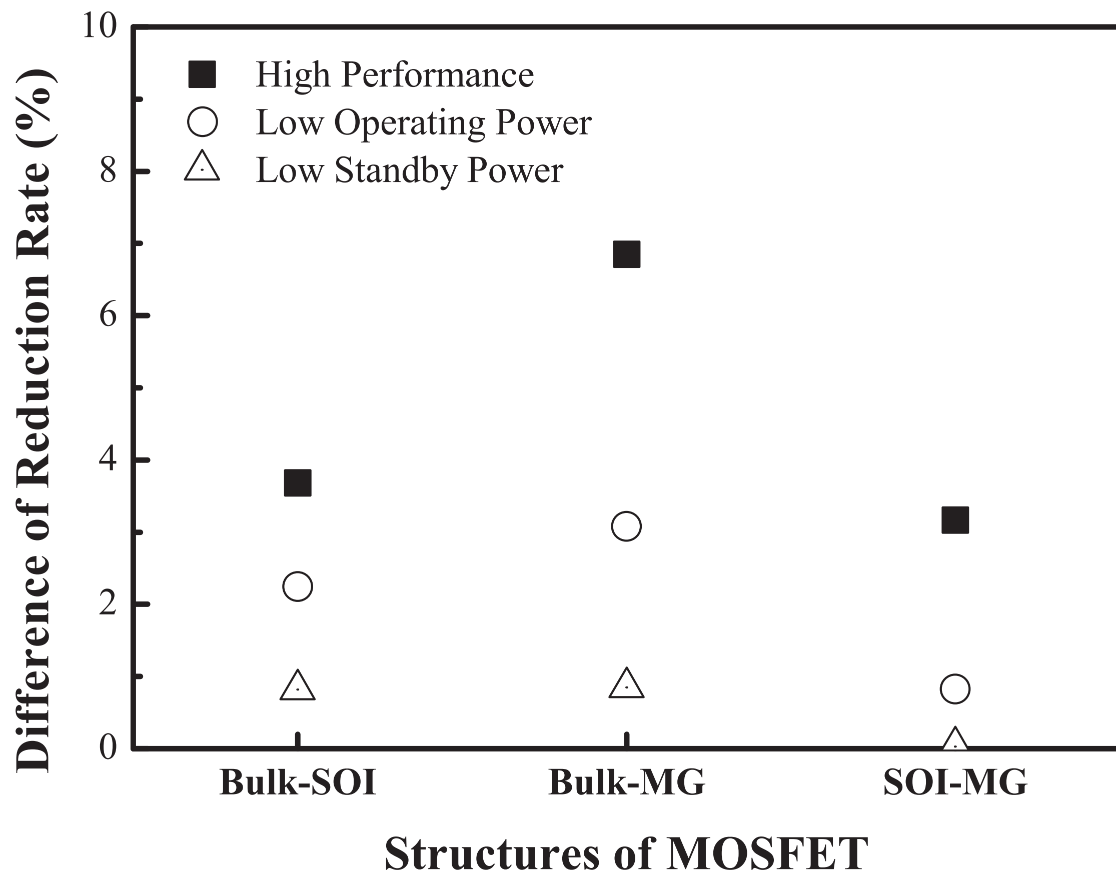


FIGURE 5.2: Difference of the reduction rates between each structure in HP, LOP, and LSTP technologies.

between bulk-SOI, bulk-MG, and SOI-MG are 0.8, 0.9, and 0.1% in LSTP technology, respectively. The differences of the reduction rate are largest in HP technology. The differences of the reduction rate between bulk-SOI and bulk-MG are above 2%, that between SOI-MG is below 1% in LOP technology. The differences of the reduction rates are below 1% in LSTP technology. The reduction rate of the saturation drain current depends on the MOSFET structure in HP and LOP technologies. The reduction rate rarely depends on the MOSFET structure in LSTP technology.

5.3 Discussion

To investigate the physical reasons underlying the reduction rate decrease as the MOSFET structure changes, expansion components of the saturation current influenced by the series resistance are analyzed. The expansion components normalized by bulk MOSFET are compared with the other components of SOI and MG in HP, LOP, and LSTP technologies.The calculated results of the expansion components are shown in Table 5.3.

Figure 5.3 shows normalized expansion components of the saturation current including an effect of the series resistance in HP technology. Normalized first components for SOI and MG are 0.96 and 0.86, respectively. Normalized second components for SOI and MG are 0.98 and 1.01, respectively. Normalized third components for SOI and MG are 0.96 and 0.93, respectively. Normalized first components for SOI and MG structures decrease compared with bulk structure. Normalized second and third components for SOI and MG structures are almost constant compared with bulk structure. In HP technology, the ratio of the series resistance to the channel resistance is the dominant factor in the reduction rate of the saturation current. The ratio decreases owing to constant series resistance and increase of the channel resistance ($R_{\mathrm{ch}} = V_{\mathrm{dd}}/I_{\mathrm{Dsat0}}$) as the MOSFET structure changes bulk to SOI and SOI to MG. The saturation current and gate oxide capacitance decrease owing to increase of the gate oxide thickness. Required gate oxide thickness increases as the MOSFET structure changes bulk to SOI and SOI to MG to control the gate leakage current.

Figure 5.4 shows normalized expansion components of the saturation current including an effect of the series resistance in LOP technology. Normalized first components for SOI and MG are 0.97 and 0.97, respectively. Normalized second components for SOI and MG are 0.94 and 0.92, respectively. Normalized third components for SOI and MG are 0.97 and 0.94, respectively. Normalized second components for SOI and MG structures decrease compared with bulk structure. Normalized first and third components for SOI

Table 5.3: Calculated expansion components of 1st-order terms in HP, LOP, and LSTP technologies.

	High Performance			Low Operating Power			Low STandby Power		
	Bulk	SOI	MG	Bulk	SOI	MG	Bulk	SOI	MG
First component	0.31	0.30	0.27	0.17	0.16	0.16	0.07	0.09	0.10
Second component	1.16	1.14	1.17	1.65	1.55	1.51	2.39	1.89	1.93
Third component	1.13	1.09	1.05	1.14	1.10	1.07	1.24	1.11	1.09

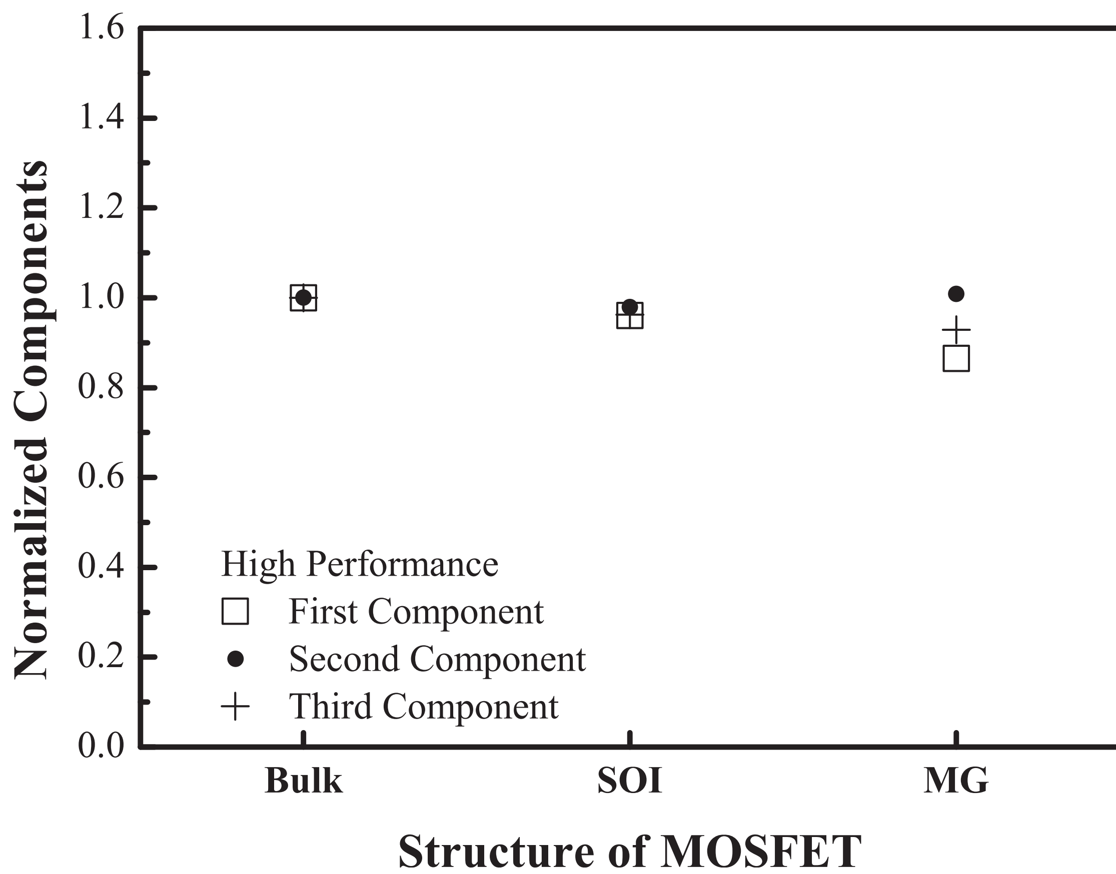


FIGURE 5.3: Normalized expansion components of the saturation current including an effect of the series resistance in HP technology.

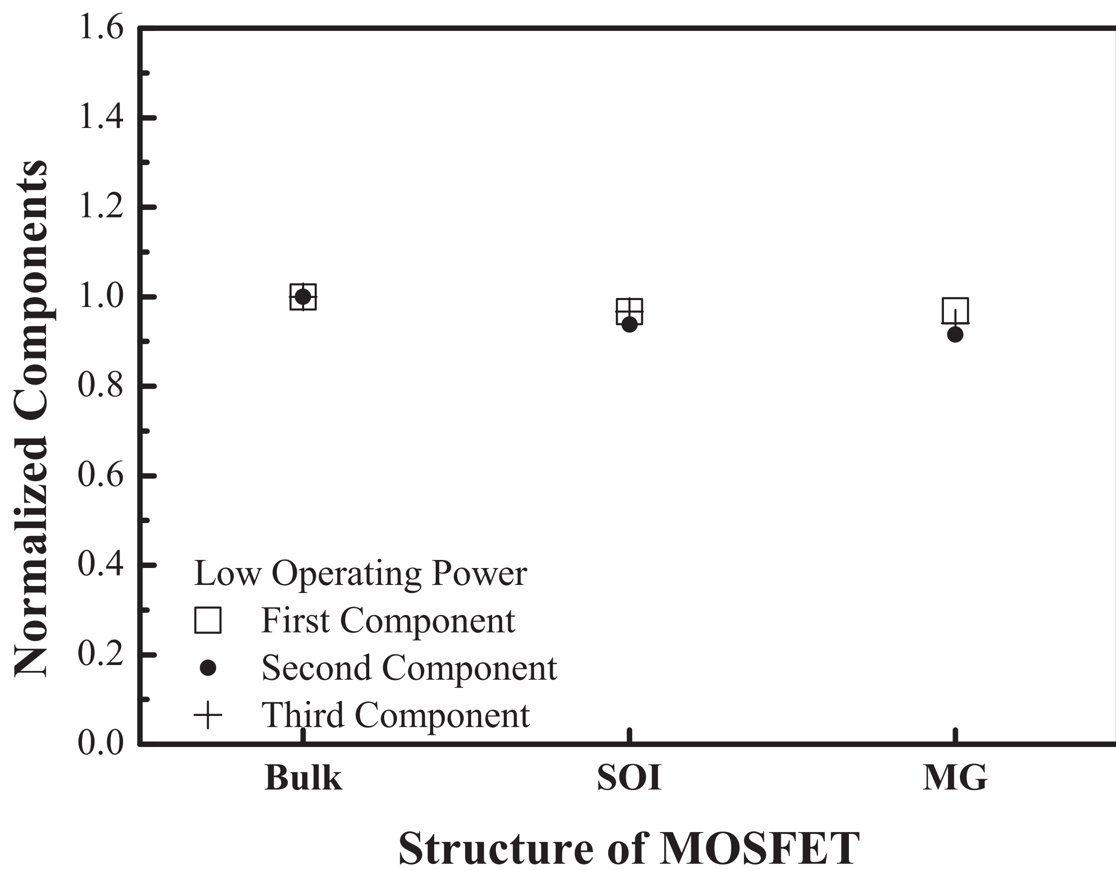


FIGURE 5.4: Normalized expansion components of the saturation current including an effect of the series resistance in LOP technology.

and MG structures are almost constant compared with bulk structure. In LOP technology, the ratio of the over-drive voltage to the supply voltage is the dominant factor in the reduction rate of the saturation current. The ratio decreases owing to constant supply voltage and increase of the overdrive voltage as the MOSFET structure changes bulk to SOI. The overdrive voltage increases owing to decrease of threshold voltage by enhancement of gate controllability. The ratio of voltages is sensitive because the supply voltage is the smallest compared to other technologies. As the MOSFET structure changes SOI to MG, the ratio of voltages is almost constant owing to the effect of the gate controllability.

Figure 5.5 shows normalized expansion components of the saturation current including an effect of the series resistance in LSTP technology. Normalized first components for SOI and MG are 1.32 and 1.32, respectively. Normalized second components for SOI and MG are 0.79 and 0.81, respectively. Normalized third components for SOI and MG are 0.90 and 0.88, respectively. Normalized first components for SOI and MG structures increase compared with bulk structure. Normalized second and third components for SOI and MG structures decrease compared with bulk structure. In LSTP technology, both the ratio of the series resistance to the channel resistance and the ratio of the overdrive voltage to the supply voltage are the dominant factors in the reduction rate of the saturation current. However, the reduction rate depends on the MOSFET structure rarely because the structural dependence is canceled by multiplying each component.

Requirements of the MOSFETs as the structure changes are different in each technology. A key transistor performance of the requirements is the intrinsic switching frequency for device design in Table 5.1. In HP technology, the MOSFETs are focused on the highest switching frequency. The transistors have both the highest device performance and the highest gate leakage current density to improve the channel resistance. The ratio of the series resistance to the channel resistance is the main factor in the saturation current. Therefore, the ratio of the series resistance to the channel resistance is important in the reduction of the saturation current by the series resistance. In LOP technology, the MOSFETs are focused on reducing of the operating power dissipation by controlling the gate leakage current and the operating current. The transistors have lower performance and lower leakage current. To effectively reduce the power dissipation, the supply voltage is minimized. The ratio of the over-drive voltage to the supply voltage is the main factor in the saturation current. Therefore, a ratio of the over-drive voltage to the supply voltage is important in the reduction of the saturation current. In LSTP technology, the MOSFETs are focused on the gate leakage current and the off-state current. The transistors have both the lowest device performance and the lowest

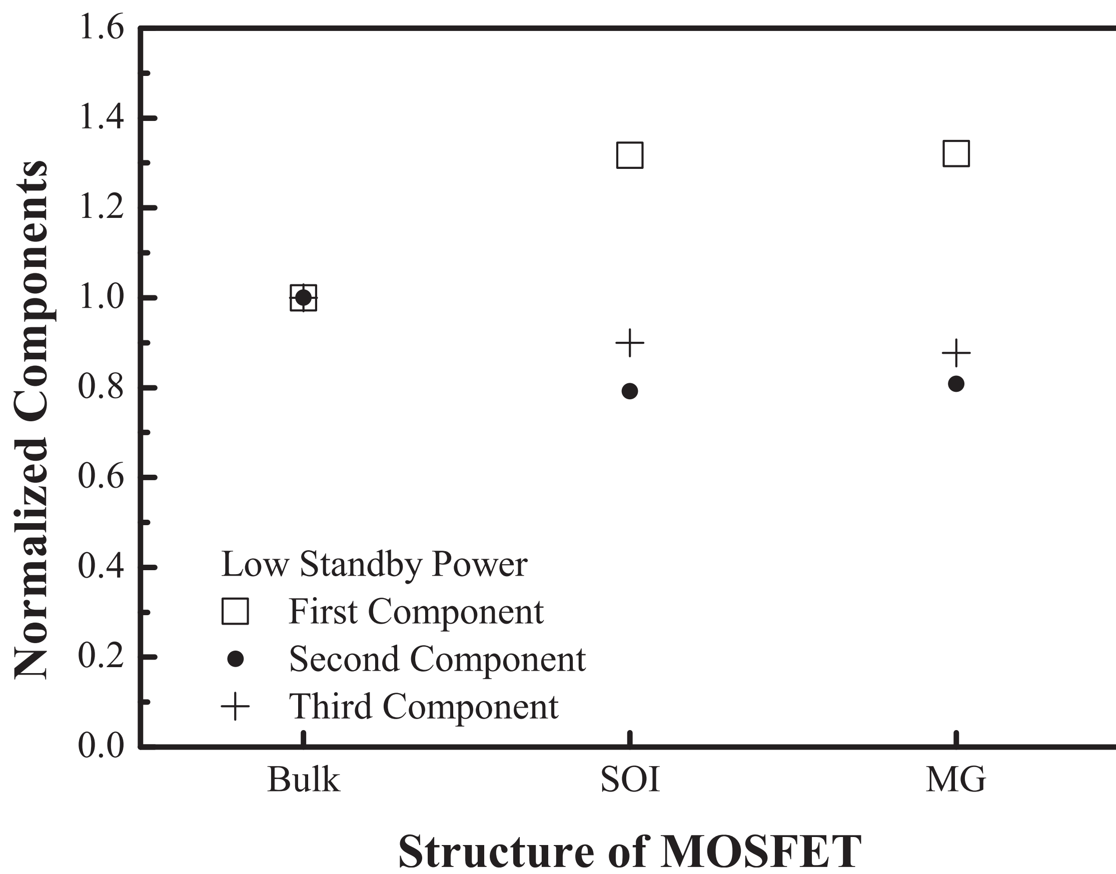


FIGURE 5.5: Normalized expansion components of the saturation current including an effect of the series resistance in LSTP technology.

gate leakage current of all. The lower voltage and higher resistance ratios are main factors in the saturation current. Therefore, the voltage and resistance ratios are important in the reduction of the saturation current.

5.4 Summary

We investigated the structural dependence of the series-resistance effect on the saturation currents in sub-20 nm MOSFETs. The saturation currents including the resistance effect were calculated using the analytic current model for bulk, SOI, and MG MOSFETs. The calculated saturation currents were compared with the intrinsic saturation currents to calculate reduction rates of the saturation current in HP, LOP, and LSTP technologies.

In HP technology, the reduction rates are 29.0, 25.3, and 22.1% for bulk, SOI, and MG MOSFETs, respectively. In LOP technology, the reduction rates are 23.8, 21.5 and 20.7% for bulk, SOI, and MG MOSFETs, respectively. In LSTP technology, the reduction rates are 17.5, 16.7, and 16.6% for bulk, SOI, and MG MOSFETs, respectively. The reduction rate of the saturation drain current depends on structures of the MOSFETs as the structure of MOSFETs changes. In HP technology, a ratio of the series resistance to the channel resistance is the dominant factor in the reduction rate of the saturation current. It is important to consider not only reducing of channel resistance by high mobility material but also reducing of the source resistance. In LOP technology, a ratio of the over-drive voltage to the supply voltage is the dominant factor in the reduction rate of the saturation current. It is important to consider not only reducing of the supply voltage but also reducing of the overdrive voltage. In LSTP technology, both the resistance and voltage ratios are dominant factors because the structural dependence is canceled by multiplying the lower third component, the lower voltage and higher resistance ratios. It is important to consider the canceling by multiplying resistance ratio and voltage ratio.

Chapter 6

Conclusions

In device design of sub-20 nm metal-oxide-semiconductor field-effect transistors (MOSFETs), an effect of source and drain series resistance on saturation drain current becomes important. To investigate the effect of series resistance, we derived an analytical model for saturation drain-current including the higher order effect of the source and drain series resistance for a sub-20nm gate length MOSFETs. Past analytical model including the effect of series resistance and the derived analytical model were introduced. To investigate the effect of the series resistance on model parameters using circuit simulation, the α power model as a simple current model for circuit simulation was introduced briefly.

The importance of source-drain resistance was tested for effect on the characteristics of the MOSFET to become increasingly important in the design and development of new devices for the future. We calculated the ratio of the overdrive voltage to the supply voltage as a function of the MOSFET structure. The change of that due to the difference of the structure is small, we found that the effect of the source and drain resistance becomes larger every year. The effects of the source-drain resistance on the MOSFET characteristics was investigated using circuit simulation. As a result, the influence of the source and drain resistance on the channel length modulation was found to be independent of the gate voltage the gate length is reduced.

We investigate the saturation drain current including the higher-order terms of the series resistance. The reduction rate of the saturation drain current influenced by the series resistance increases from 15.8 to 24.0% as the gate length decreases from 32 to 18 nm. To investigate the higher-order terms of the series resistance, we calculate component ratios of the higher order terms. The component ratios of 1st-order and 2nd-order terms change from 80.7 to 68.6% and from 15.6 to 22.0% as the gate length decreases from 32 to 18 nm, respectively. We find that the higher order terms are

indispensable for analyzing the effect of the series resistance as the gate length decreases. From the analysis of the normalized expansion components, the increase in the ratio of the source resistance to the channel resistance leads to that in reduction rate. This implies that the resistance ratio of the source resistance to the channel resistance is a dominant factor in device design and development for sub-20 nm MOSFETs.

We investigate the saturation drain current including the effects of the series resistance for sub-20 nm bulk, SOI, and MG MOSFETs in HP, LOP, and LSTP technologies. A reduction rate of the saturation drain current by the series resistance is calculated. In HP technology, the reduction rates are 29.0, 25.3, and 22.1% for bulk, SOI, and MG MOSFETs, respectively. In LOP technology, the reduction rates are 23.8, 21.5 and 20.7% for bulk, SOI, and MG MOSFETs, respectively. In LSTP technology, the reduction rates are 17.5, 16.7, and 16.6% for bulk, SOI, and MG MOSFETs, respectively. The reduction rate of the saturation drain current depends on the change in MOSFET structure. In HP technology, the dominant factor in reduction rate of the saturation drain current is $R_{\mathrm{s}}/R_{\mathrm{ch}}$. It is important to consider not only reducing of channel resistance by high mobility material but also reducing of the source resistance. In LOP technology, the dominant factor in reduction rate of the saturation drain current is $V_{\mathrm{dd}}/V_{\mathrm{gt}}$. It is important to consider not only reducing of the supply voltage but also reducing of the overdrive voltage. In LSTP technology, the dominant factors in reduction rate of the saturation drain current are $R_{\mathrm{s}}/R_{\mathrm{ch}}$ and $V_{\mathrm{dd}}/V_{\mathrm{gt}}$. It is important to consider the canceling by multiplying resistance ratio and voltage ratio.

Reference

[1] Y. Taur and T. H. Ning: *Fundamentals of Modern VLSI Devices* (Cambridge University Press, New York, 1998) Chap. 3.

[2] Y. Taur , G. J. Hu , R. H. Dennard , L. M. Terman , C.-Y. Ting, and K. E. Petrillo "A self-aligned 1-μm-channel CMOS technology with retrograde n-Well and thin epitaxy," IEEE Journal of Solid-State Circuits, vol. 20, pp. 123 -129, 1985.

[3] A. N. Broers and R. H. Dennard, "Impact of electron beam technology on silicon device fabrication," Semicond. Silicon (Electrochem. Soc. Publication), H. R. Huff and R. R. Burgess, eds., pp. 830 –841, 1973.

[4] R. H. Dennard, F. H. Gaensslen, L. Kuhn, and H. N. Yu, "Design of micron MOS switching devices," in IEDM Tech. Dig., pp. 168 -170, 1972.

[5] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," IEEE J. Solid-State Circuits, vol. 9, pp. 256 -268, 1974.

[6] G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to a 1/4 micrometer MOSFET design," IEEE Trans. Electron Devices, vol. ED-31, pp. 452 -462, 1984.

[7] C. F. Codella and S. Ogura "Halo doping effects in submicron DI-LDD device design", Int. Electron Devices Meeting, vol. 31, pp. 230 -233, 1985.

[8] J. Welser, J. L. Hoyt, and J. F. Gibbons, "Electron mobility enhancementin strained-Si n-type metal-oxide-semiconductor field-effect transistors," IEEE Electron Device Lett., vol. 15, no. 3, pp. 100 –102, 1994.

[9] L. A. Akers, M. A. Holly, and C. Lund, "Hot carriers in small geometry CMOS," in IEDM Tech. Dig., pp. 80 -83, 1984.

[10] S. Ogura, C. F. Codella, N. Rovedo, J. F. Shepard, and J. Riseman, "A half micron MOSFET using double implanted LDD," in IEDM Tech. Dig., pp. 718 -721, 1982.

[11] J. Maserjian, "Tunneling in thin MOS structures," J. Vac. Sci. Technol., vol. 11, no. 6, pp. 996 –1003, 1974.

[12] S. Lo, D. Buchanna, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from inversion layer of ultrathin oxide nMOSFETs," IEEE Electron Device Lett., vol. 18, pp. 209 -210, 1997.

[13] T. Morimoto, H. Momose , Y. Ozawa, K. Yamabe, and H. Iwai "Effects of boron penetration and resultant limitations in ultra thin pure-oxide and nitrided-oxide gate-films," in IEDM Tech. Dig., pp. 429 -432, 1990.

[14] E. P. Gusev, M. Copel, E. Cartier, I. J. R. Baumvol, C. Krug, and M. A. Gribelyuk, "High-resolution depth profiling in ultrathin Al2O3 on Si," Appl. Phys. Lett., vol. 76, pp.176 -178, 2000.

[15] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, "Fermi-level pinning at the polySi/metal oxide interface," in Symp. VLSI Tech. Dig., pp. 9 -10, 2003.

[16] V. Misra, G. Lucovsky, and G. Parsons, "Issues in High-k Gate Stack Interfaces," MRS Bull., vol. 27, no. 3, pp. 212-216, 2001.

[17] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo, "Review on high-κ dielectrics reliability issues," IEEE Trans. Device Mater. Rel., vol. 5, no. 1, pp.5 -19, 2005.

[18] J. P. Colinge "Subthreshold slope of thin film SOI MOSFET's," IEEE Electron Device Lett., vol. EDL-7, pp. 244 -246, 1986.

[19] J. P. Colinge "Reduction of kink effect in thin-film SOI MOSFETs," IEEE Electron Device Lett., vol. 9, pp. 97 -99, 1988.

[20] W. Haensch, E. J. Nowak, R. H. Dennard, P. M. Solomon, A. Bryant, O. H. Dokumaci, A. Kumar, X. Wang, J. B. Johnson, and M. V. Fischetti, "Silicon CMOS devices beyond scaling," IBM J. Res. Develop., vol. 50, no. 4/5, pp. 339 -361, 2006.

[21] Q. Liu , A. Yagishita , N. Loubet , A. Khakifirooz , P. Kulkarni , T. Yamamoto , K. Cheng , M. Fujiwara , J. Cai , D. Dorman , S. Mehta , P. Khare , K. Yako , Y. Zhu , S. Mignot , S. Kanakasabapathy , S. Monfray , F. Boeuf , C. Koburger , H. Sunamura , S. Ponoth , A. Reznicek , B. Haran , A. Upham , R. Johnson , L. F. Edge , J. Kuss , T. Levin , N. Berliner , E. Leobandung , T. Skotnicki , M. Hane , H. Bu , K. Ishimaru , W. Kleemeier , M. Takayanagi , B. Doris and R. Sampson "Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22 nm node and beyond," in VLSI Symp. Tech. Dig., pp. 61 -62, 2010.

[22] A. Majumdar, Z. Ren, S. J. Koester, and W. Haensch, "Undoped-body extremely thin SOI MOSFETs with back gates," IEEE Trans. Electron Devices, vol. 56, no. 10, pp. 2270 –2276, 2009.

[23] Roadmap of 2007 edition can be downloaded from the following URL; http://www.itrs.net/Links/2007ITRS/Home2007.htm.

[24] M. Bohr "The evolution of scaling from the homogeneous era to the heterogeneous era," in IEDM Tech. Dig., pp. 1 -6, 2011.

[25] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," Proc. IEEE, vol. 91, no. 2, pp. 305 -327, 2003.

[26] N. Tega, H. Miki, F. Pagette, D. J. Frank, A. Ray, M. J. Rooks, W. Haensch, and K. Torii "Increasing Threshold Voltage Variation due to Random Telegraph Noise in FETs as Gate Lengths Scale to 20 nm," in VLSI Symp. Tech. Dig., pp. 51 -52, 2009.

[27] A. Dixit, A. Kottantharayil, N. Collaert, M. Goodwin, M. Jurczak, and K. D. Meyer, "Analysis of the parasitic S/D resistance in multiple-gate FETs," IEEE Trans. Electron Devices, vol. 52, no. 6, pp. 1132 -1140, 2005.

[28] K. Kuhn, "Considerations for ultimate CMOS scaling," IEEE Trans. Electron Dev., vol. 59, no. 7, pp.1813 -1828, 2012.

[29] K. K. Ng and W. T. Lynch, "Analysis of the gate-voltage-dependent series resistance of MOSFET's", IEEE Trans. Electron Devices, vol. ED-33, no. 7, pp.965 1986.

[30] F. Schwierz, H. Wong and J. J. Liou: *Nanometer CMOS* (Pan Stanford Publishing, Singapore, 2010) Chap. 1.

[31] K. K. Ng and W. T. Lynch, "The impact of intrinsic series resistance on MOSFET scaling," IEEE Trans. Electron Devices, vol. 34, no. 3, pp. 503 -511, 1987.

[32] R. Izawa, T. Kure, S. Iijima, and E. Takeda, "The impact of gate-drain overlapped LDD (GOLD) for deep submicron VLSI's," in IEDM Tech. Dig., pp.38, 1987.

[33] A. Hamada, Y. Igura, R. Izawa, and E. Takeda, "N source/drain compensation effects in submicrometer LDD MOS devices," IEEE Electron Device Lett., vol. 8, no. 9, pp.398 -, 1987.

[34] Y. Mii, S. Rishton, Y. Taur, D. Kern, T. Lii, K. Lee, K. A. Jenkins, D. Quinlan, T. Brown Jr., D. Danner, F. Sewell, and M. Polcari, "Experimental high performance sub-0.1 μm channel nMOSFET's," IEEE Electron Device Lett., vol. 15, pp. 28 -30, 1994.

[35] T.-Y. Liow, K.-M. Tan, R. T. P. Lee, A. Du, C.-H. Tung, G. S. Samudra, W.-J. Yoo, N. Balasubramanian, and Y.-C. Yeo, "Strained n-channel FinFETs with 25 nm gate length and silicon–carbon source/drain regions for performance enhancement," in Symp. VLSI Tech., pp. 56 –57, 2006.

[36] Q. Liu, F. Monsieur, A. Kumar, T. Yamamoto, A. Yagishita, P. Kulkarni, S. Ponoth, N. Loubet, K. Cheng, A. Khakifirooz, B. Haran, M. Vinet, J. Cai, J. Kuss, B. Linder, L. Grenouillet, S. Mehta, P. Khare, N. Berliner, T. Levin, S. Kanakasabapathy, A. Upham, R. Sreenivasan, Y. Le Tiec, N. Posseme, J. Li, J. Demarest, M. Smalley, E. Leobandung, S. Monfray, F. Boeuf, T. Skotnicki, K. Ishimaru, M. Takayanagi, W. Kleemeier, H. Bu, S. Luning, T. Hook, M. Khare, G. Shahidi, B. Doris, and R. Sampson, "Impact of Back Bias on Ultra-Thin Body and BOX (UTBB) Devices," in Symp. VLSI Tech., pp. 160 -161, 2011.

[37] J. Widiez, J. Lolivier, M. Vinet, T. Poiroux, B. Previtali, F. Dauge, M. Mouis, and S. Deleonibus, "Experimental evaluation of gate architecture influence on DG SOI MOSFETs performance", IEEE Trans. Electron Devices, vol. 52, no. 8, pp. 1772 -1779, 2005.

[38] Available at http://www.intel.com/technology/architecture-silicon/22nm/

[39] N. D. Arora, R. Rios, C.-L. Huang, and K. Raol, "PCIM: A Physically based continuous short-channel IGFET model for circuit simulation," IEEE Trans. on Electron Dev., vol. 41, no. 6, pp. 988 -997, 1994.

[40] F.M. Klaassen, P.T.J. Biermans, and R.M.D. Velghe, "The Series Resistance of Submicron MOSFETs and its Effect on their Characteristics," ESSDERC, C4, pp. 257 -260, 1988.

[41] J. B. Roldán, F. Gámiz, J. A. Lopez-Villanueva, P. Cartujo, and J. E. Car-celler, "A model for the drain current of deep submicrometer MOSFET's including electron-velocity overshoot," IEEE Trans. Electron Devices, vol. 45, no. 10, pp.2249 -2251, 1998.

[42] K. Y. Toh, P. K. Ko, and R. G. Meyer, "An engineering model for short-channel MOS devices," IEEE J. Solid-State Circuits, vol. 23, no. 4, pp.950 -958, 1988.

[43] M.C. Jeng, J. E. Chung, P. K. Ko, and C. Hu, "The effects of source/drain resistance on deep submicrometer device performance," IEEE Trans. Electron Devices, vol. 37, no. 11, pp. 2408 -2410, 1990.

[44] K. Chen, H. Wann, J. Duster, D. Pramanik, S. Nariani, P. Ko, and C. Hu, "An accurate semi-empirical saturation drain current model for LDD N-MOSFET," IEEE Electron Device Lett., vol. 17, no. 3, pp.145 -147, 1996.

[45] K. Chen, J. Duster, H. C. Wann, T. Tanaka, M. Yoshida, P. K. Ko, and C. Hu, "Universal MOSFET carrier mobility model explicitly based on V_{t}, V_{g}, and t_{ox} and its application in device modeling and optimization," Proc. 1995 Int. Semiconduct. Dev. Res. Conf., pp.607 -610, 1995.

[46] T. Skotnicki, C. Denat, P. Senn, G. Merckel, and B. Hennion, “A new analog/digital CAD model for sub-halfmicron MOSFETs,” in IEDM Tech. Dig., pp. 165 -168, 1994.

[47] T. Skotnicki, “Heading for decananometer CMOS—Is navigation among icebergs still a viable strategy?,” Proc. 30th ESSDERC, pp. 19 -33, 2000.

[48] T. Skotnicki, C. Fenoulillet-Beranger, C. Gallon, F. Buf, S. Monfray, F. Payet, A. Pouydebasque, M. Szczap, A. Farcy, F. Arnaud, S. Clerc, M. Sellier, A. Cathignol, J.-P. Schoellkopf, E. Perea, R. Ferrant, and H. Mingam, “Innovative materials, devices, and CMOS technologies for low-power mobile multimedia,” IEEE Trans. Electron Devices, vol. 55, no. 1, pp.96 -130, 2008.

[49] Available at http://www.itrs.net/models.html.

[50] T. Skotnicki, F. Boeuf, H. Huff, and D. Gilmer: *High-K Gate Dielectric Materials for VLSI MOSFET Applications* (Springer-Verlag, Germany, 2005) Chap. 6.

[51] D. Munteanu and JL Autran, “Two-dimensional modeling of quantum ballistic transport in ultimate double-gate SOI devices,” Solid-State Electronics, 47, 1219-1225, 2003.

[52] H. K. Lim and J. G. Fossum, “Threshold Voltage of Thin-Film Silicon-on-Insulator (SOI) MOSFET’s,” IEEE Trans. Electron Devices, vol. 30, no. 10, pp. 1244 -1251, 1983.

[53] F. Schwierz, H. Wong and J. J. Liou: *Nanometer CMOS* (Pan Stanford Publishing, Singapore, 2010) Chap. 2.

[54] H.-Y. Chen, C.-Y. Chang, C.-C. Huang, T.-X. Chung, S.-D. Liu, J.-R. Hwang, Y.-H. Liu, Y.-J. Chou, H.-J. Wu, K.-C. Shu, C.-K. Huang, J.-W. You, J.-J. Shin, C.-K. Chen, C.-H. Lin, J.-W. Hsu, B.-C. Perng, P.-Y. Tsai, C.-C. Chen, J.-H. Shieh, H.-J. Tao, S.-C. Chen, T.-S. Gau, and F.-L. Yang, “Novel 20nm Hybrid SOI/Bulk CMOS Technology with 0.183μm^2 6T-SRAM Cell by Immersion Lithography,” in VLSI Symp. Tech. Dig., pp. 16 -17, 2005.

[55] T. Sakuirai and R. Newton, “A simple MOSFET Model for Circuit Analysis,” IEEE Trans. Electron Devices, vol. 38, no. 4, pp. 887 -894, 1991.

[56] A. Yamate, A. Hiroki, and M. Yamada, “A Simple MOSFET Model for 20nm MOS Circuit Design,” IEICE Trans. Electron., vol. J90-C, no. 4, pp. 363 -369, 2007.(in Japanese)

[57] International Technology Roadmap for Semiconductors, 2009 Edition, Process Integration, Devices, and Structures, High-performance Logic Technology Requirements

[58] T. Sakurai and A. R. Newton, “Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas,” IEEE J. Solid-State Circuits, vol. SC-25, no.2, pp. 584 -594, 1990.

[59] T. Sakurai and A. R. Newton, “A Simple MOSFET model for circuit analysis,” IEEE Trans. Electron Devices, vol.38, no. 4, pp. 887 -894, 1991.

[60] S.-D. Kim, C.-M. Park, and J. C. S. Woo: “Advanced model and analysis for series resistance in sub-100 nm CMOS including poly depletion and overlap doping gradient effect,” in IEDM Tech. Dig., pp. 723 -726, 2000.

[61] S.-D. Kim, C.-M. Park, and J. C. S. Woo: “Advanced Model and Analysis of Series Resistance for CMOS Scaling Into Nanometer Regime—Part II: Quantitative Analysis,” IEEE Trans. Electron Devices, vol. 49, no. 3, pp. 467 -472, 2002.

[62] D. A. Antoniadis, “MOSFET scalability limits and new frontier devices,” in VLSI Symp. Tech. Dig., pp. 2 -5, 2002.

[63] L. Chang, Y.-K. Choi, D. Ha, P. Ranade, S. Xiong, J. Bokor, C. Hu, and T.-J. King, “Extremely scaled silicon nano-CMOS devices,” Proc. IEEE, vol. 91, no. 11, pp. 1860 -1873, 2003.

[64] D. J. Frank, S. E. Laux, and M. V. Fischetti, “Monte Carlo simulation of a 30 nm dual-gate MOSFET: how short can Si go?,” in IEDM Tech. Dig., pp. 553 -556, 1992.

[65] J. Kedzierski, M. Ieong, E. Nowak, T. S. Kanarsky, Y. Zhang, R. Roy, D. Boyd, D. Fried, and H.-S. P. Wong, “ Extension and source/drain design for high-performance FinFET devices,” IEEE Trans. Electron Devices, vol. 50, no. 4, pp. 952 -958, 2003.

[66] H. Kawasaki, V. S. Basker, T. Yamashita, C.-H. Lin, Y. Zhu, J. Faltermeier, S. Schmitz, J. Cummings, S. Kanakasabapathy, H. Adhikari, H. Jagannathan, A. Kumar, K. Maitra, J. Wang, C.-C. Yeh, C. Wang, M. Khater, M. Guillorn, N. Fuller, J. Chang, L. Chang, R. Muralidhar, A. Yagishita, R. Miller, Q. Ouyang, Y. Zhang, V. K. Paruchuri, H. Bu, B. Doris, M. Takayanagi, W. Haensch, D. McHerron, J. O’Neill, and K. Ishimaru, “Challenges and solutions of FinFET integration in an SRAM cell and a logic circuit for 22 nm node and beyond,” in IEDM Tech. Dig., pp. 1 -4, 2009.

[67] T. Matsukawa, S. Ouchi, K. Endo, Y. Ishikawa, H. Yamauchi, Y. X. Liu, J. Tsukada, K. Sakamoto, and M. Masahara, “Comprehensive Analysis of Variability Sources of FinFET Characteristics,” in VLSI Symp. Tech. Dig., pp. 118 -119, 2009.

[68] T. C. Hsiao, N. A. Kistler, and J. C. S. Woo, “Modeling the I-V characteristics of fully depleted submicrometer SOI MOSFET’s,” IEEE Electron Device Lett., vol. 15, no. 2, pp. 45 -47, 1994.

[69] K. Chen, H. C. Wann, P. K. Ko, and C. Hu, "The impact of device scaling and power supply change on CMOS gate performance," IEEE Electron Device Lett., vol. 17, no. 5, pp. 202 -204, 1996.

[70] J. B. Roldán, F. Gámiz, J. A. López-Villanueva, and P. Cartujo-Cassimello, "Deep submicrometer SOI MOSFET drain current model including series resistance, self-heating and velocity overshoot effects," IEEE Electron Device Lett., vol. 21, no. 5, pp. 239 -241, 2000.

[71] A. Khakifirooz, O. M. Nayfeh, and D. Antoniadis, "A Simple Semiempirical Short-Channel MOSFET Current–Voltage Model Continuous Across All Regions of Operation and Employing Only Physical Parameters," IEEE Trans. Electron Devices, vol. 56, no. 8, pp. 1674 -1680, 2009.

[72] J.-C. Guo, S. S.-S. Chung, and C. C.-H. Hsu, "A new approach to determine the effective channel length and the drain-and-source series resistance of miniaturized MOSFET's," IEEE Trans. Electron Devices, vol. 41, no. 10, pp. 1811 -1818, 1994.

[73] M.-C. Hu and S.-L. Jang, "An analytical fully-depleted SOI MOSFET model considering the effects of self-heating and source/drain resistance," IEEE Trans. Electron Devices, vol. 45, no. 4, pp. 797 -801, 1998.

[74] H. K. Lim and X. Zhou, "A Physically-Based Semi-Empirical Series Resistance Model for Deep-Submicron MOSFET I-V Modeling," IEEE Trans. Electron Devices, vol. 47, no. 6, pp. 1300 -1302, 2000.

[75] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Trans. Electron Devices, vol. 47, no. 12, pp. 2320 -2325, 2000.

[76] D. Hisamoto, T. Kaga, and E. Takeda, "Impact of the vertical SOI 'DELTA' structure on planar device technology," IEEE Trans. Electron Devices, vol. 38, no. 6, pp. 1419 -1424, 1991.

[77] C. H. Wann, K. Noda, T. Tanaka, M. Yoshida, and C. Hu, "A comparative study of advanced MOSFET concepts," IEEE Trans. Electron Devices, vol. 43, no. 10, pp. 1742 -1753, 1996.

[78] H.-S. P. Wong, "Beyond the conventional transistor," IBM J. Res. Dev., vol. 46, no. 2/3, pp. 133 -168, 2002.

[79] C. H. Choi, J. S. Goo, Z. Yu, and R. W. Dutton, "Shallow source/drain extension effects on external resistance in sub-0.1 μm MOSFETs," IEEE Trans. Electron Devices, vol. 47, no. 3, pp. 655 -658, 2000.

[80] X. Wang, P. Oldiges, A. Bryant, J. Cai, Q. Ouyang, and K. Rim, "Simulation Analysis of Series Resistance for SOI MOSFET in Nanometer Regime," in SISPAD, pp. 239 -242, 2005.

[81] S. Thompson, M. Alavi, R. Arghavani, A. Brand, R. Bigwood, J. Brandenburg, B. Crew, V. Dubin, M. Hussein, P. Jacob, C. Kenyon, E. Lee, B. Mcintyre, Z. Ma, P. Moon, P. Nguyen, M. Prince, R. Schweinfurth, S. Sivakumar, P. Smith, M. Stettler, S.Tyagi, M. Wei, J. Xu, S. Yang, and M. Bohr, "An enhanced 130 nm generation logic technology featuring 60 nm transistors optimized for high performance and low power at 0.7 - 1.4 V," in IEDM Tech. Dig., pp. 11.6.1 -11.6.4, 2001.

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List of Publications

1. J. C. Yoon, Y. Nakade, A. Hiroki, F. Inoue and K. Tomiyama, “Effects of Source and Drain Resistances on Analytical Model Parameters for 20 nm MOSFETs,” IEEJ C, vol. 131-11, pp. 1833 -1837, 2011.(in Japanese)

2. J.C. Yoon, A. Hiroki, and K. Kobayashi, “Higher-Order Effect of Source–Drain Series Resistance on Saturation Drain Current in Sub-20 nm Metal– Oxide– Semiconductor Field-Effect Transistors,” Japanese Journal of Applied Physics, vol. 51, 111101, 2012.

3. J.C. Yoon, A. Hiroki, and K. Kobayashi, “Structural Dependence of Source-and-Drain Series Resistance on Saturation Drain Current for Sub-20 nm Metal– Oxide–Semiconductor Field-Effect Transistors,” Japanese Journal of Applied Physics, vol. 52, 071302, 2013.

List of Presentations

First Author

1. J. C. Yoon, A. Hiroki, T. Sano, K. Kobayashi, "An Estimation of Saturation Current Influenced by Source and Drain Resistances for Sub-20 nm MOSFETs," International Meeting for Future of Electron Devices, Kansai, pp. 56 -57, 2011.

2. J. C. Yoon, A. Hiroki and K. Kobayashi, "An Estimation of Analytical Saturation Drain Current Model Including Higher-Order effects of Source/Drain Resistances for Gate Length Sub-20 nm MOSFET," Kansai-section Joint Convention of Institutes of Electrical Engineering, G6 30P4-16, 2011. (in Japanese)

3. J. C. Yoon and A. Hiroki, "Higher-order Effects of Source and Drain Parasitic Resistances for Nanoscale MOSFETs," IEICE Technical Report STM, No. 141, pp. 77 -81, 2011. (in Japanese)

4. J. C. Yoon, A. Hiroki, and K. Kobayashi, "Structure Dependence of Reduced Saturation Current Influenced by Source and Drain Resistances for 17 nm MOSFETs," International Meeting for Future of Electron Devices, Kansai, pp. 92 -93, 2012.

5. J. C. Yoon and A. Hiroki, "A Study of Effects of Source/Drain Parasitic Resistance on Parameters of Analytical Drain Current Model for 20 nm MOSFETs," National Convention of the Institute of Electronics Engineers of Korea, vol. 1-1, pp. 15 -18, 2012. (in Korean)

Co-Author

1. A. Hiroki and J. C. Yoon, “Gate Voltage Dependence of Channel Length Modulation Coefficient for Nanoscale MOSFETs,” IEICE Technical Report STM, no. 141, pp. 71 -76, 2011.(in Japanese)

2. M. Yamamoto, A. Hiroki, and J. C. Yoon, “An Estimation of the Carrier Mobility Model Influenced by Inversion Charge Confinement for Sub-20nm MOSFETs,” IEICE Technical Report STM, no. 290, pp. 25 -30, 2012.(in Japanese)

3. M. Yamamoto, A. Hiroki, and J. C. Yoon, “An Estimation of the Inversion Charge Influenced by Quantum Effect for Sub-20nm MOSFETs,” International Meeting for Future of Electron Devices, Kansai, pp. 90 -91, 2012.

4. M. Yamamoto, A. Hiroki, and J. C. Yoon, “An Estimation of the Effective Mobility Influenced by Quantum Effect for Sub-20nm MOSFETs,” Kansai-section Joint Convention of Institutes of Electrical Engineering, G6 8AMD-4, 2012.(in Japanese)

5. Y. Goto, A. Hiroki, A. Matsuda, M. Nakamura, and J.C. Yoon, “Gate Voltage Dependence of Channel Length Modulation for Ge p-channel MOSFETs,” International Meeting for Future of Electron Devices, Kansai, pp. 40 -41, 2014.

6. A. Matsuda, A. Hiroki, Y. Goto, M. Nakamura, and J.C. Yoon, “Gate Voltage Dependence of Channel Length Modulation for InGaAs n-channel MOSFETs,” International Meeting for Future of Electron Devices, Kansai, pp. 44 -45, 2014.